DESIGN OF ULTRA LOW POWER CIRCUITS USING NANO-SCALE HYBRID TECHNOLOGY

A THESIS SUBMITTED TO
SAVITRIBAI PHULE PUNE UNIVERSITY

FOR AWARD OF DEGREE OF
DOCTOR OF PHILOSOPHY (PH.D.)
IN THE FACULTY OF
SCIENCE AND TECHNOLOGY
(ELECTRONICS AND TELECOMMUNICATION ENGINEERING)

SUBMITTED BY
SANDIP BHAGWAT RAHANE

UNDER THE GUIDANCE OF
DR. ABDUL KADIR KURESHI

RESEARCH CENTRE
MATOSHRI COLLEGE OF ENGINEERING AND RESEARCH CENTRE,
Eklahare, Nashik, (M.S.), India, Pin: 422 105

DECEMBER 2018

CERTIFICATE OF THE GUIDE

Certified that the work incorporated in the thesis **"Design of Ultra Low Power Circuits Using Nano-scale Hybrid Technology",** submitted by **Mr. Sandip Bhagwat Rahane,** was carried out by the candidate under my supervision/ guidance. Such material has been obtained from other sources has been duly acknowledged in the thesis.

Date:

Dr. A. K. Kureshi
Research Guide

DECLARATION

I declare that the thesis entitled **“Design of Ultra Low Power Circuits Using Nano-scale Hybrid Technology”,** submitted by me for the degree of Doctor of Philosophy is the record of work carried out by me during the period from 13/09/2013 to 04/09/2018 under the guidance of **Dr. A. K. Kureshi** and has not formed the basis for the award of any degree, diploma, associateship, fellowship, titles in this or any other University or other institution of Higher learning.

I further declare that the material obtained from other sources has been duly acknowledged in the thesis.

Date: **Sandip Bhagwat Rahane**

ACKNOWLEDGEMENTS

There are countless individuals that deserve my sincere gratitude for helping me complete this work. First and foremost, I would like to express my profound gratitude to my mentor and guide **Dr. A. K. Kureshi,** for his innovative ideas, constructive guidance, and expert advice. His advice, expertise and research attitude made the job of completing this thesis lot easier than it would have been. His observations and comments helped me to channelize the research in proper direction. He was always available for his valuable suggestions and critical evaluation of this work. For this and much more, I am deeply indebted to him.

I would like to thank from the bottom of my heart, **Dr. G. K. Kharate**, Principal, Matoshri College of Engineering and Research Center for providing me the timely guidance, key inputs and expert advice. I am very thankful to **Dr. J. J. Chopade** for his words of encouragement and guidance which have improved the quality of this work tremendously. Special thanks to **Prof. D. D. Dighe,** Head of the Department, for his valuable guidance. Thanks to all past and present colleagues and friends, **Dr. S. D. Pable**, **Prof. D. D. Ahire, Prof. M. P. Dongare, Prof. R.B. Sathe, Prof. S.K. Chaudhary and Prof. D. A. Mhaske** for their valuable support and insightful suggestions.

My sincere thanks goes to Management and Principal of my parent institute Amrutvahini Sheti and Shikshan Vikas Sanstha's, Amrutvahini College of Engineering, Sangamner for providing flexibility required to carry out this research work.

I would like to thank my brothers, **Dr**. **Suhas** and **Dr. Santosh** for their unselfish love and encouragement. I would like to acknowledge the unconditional love, moral and spiritual support of my dear parents, **Mrs. Anusaya** and **Mr. Bhagwat Rahane.** I take this great opportunity to thank my beloved wife **Mrs. Seema** from the bottom of my heart for her love, patience and understanding. Last but not the least, I am extremely thankful to my cute and loving kids **Piyush** and **Anushri**. I feel blessed to have such a wonderful family.

I would like to thank everyone else; whose names have skipped mention. Thank you everyone!!!

Sandip Bhagwat Rahane

ABSTRACT

Advances in the field of nano-electronics are playing a vital role in the overall human development and will continue to do so in a longer time horizon. One of the significant development in the field of nanoelectronics is the research contributing to the development of extended/beyond CMOS transistors which will potentially overcome limitations posed by conventional CMOS transistors. Carbon Nanotube Field Effect Transistor (CNFET) is amongst the several contenders that will either possibly substitute CMOS transistors or can be used in concurrence with CMOS in a hybrid manner. One of the approaches for effective utilization of these extended/beyond CMOS devices is to have hybrid circuits such as hybrid CMOS-CNFET circuits.

This research work used SPICE models and simulations to investigate hybrid CMOS-CNFET circuits in a complementary manner. Another aspect of this research work is to reduce the power consumption of these hybrid nanoelectronics circuits. Following circuits were investigated with a hybrid approach: Hybrid CMOS-CNFET Voltage Controlled Oscillator (VCO), Hybrid CMOS-CNFET OTA-C filters, Hybrid bandgap reference circuit, and a Dual threshold two transistor voltage reference circuit.

The hybrid VCO exhibited improved linear response over a broad control voltage range with a significant reduction in power dissipation. The hybrid OTA-C filters satisfied ultra-low-power consumption as well as low-frequency cutoffs suitable for signal processing applications dealing with very slow or low-frequency electrical activities of the biomedical signals. The first order low pass filter consumes 216nW, the second order low pass filter consumes 433nW, and second order notch filter consumes 431nW while the fifth order elliptic filter consumes 1.47μW. Hybrid bandgap reference circuit confirmed its robustness against variations in temperature and power supply with low power dissipation. The dual threshold voltage reference circuit exploited subthreshold conduction and threshold voltage difference between two CNFETs to achieve ultra-low power consumption of just 3.42pW.

TABLE OF CONTENTS

Acknowledgements……………………………………………………….. **i**

Abstract………………………………………………………………… **ii**

Table of Contents………………………………………………………. **iii**

List of Figures…………………………………………………………. **vii**

List of Tables………………………………………………………….. **xi**

List of Symbols………………………………………………………. **xiii**

List of Abbreviations………………………………………………... **xvii**

1. Introduction…………………………………………………………. **1**

1.1 Overview…………………………………………………………. **1**

1.2 Motivation……………………………………………………….... **3**

1.3 Objectives of Research…………………………………………… **3**

1.4 Nanoelectronics…………………………………………………... **4**

1.4.1 Extended CMOS and Beyond CMOS Devices………….. **6**

1.4.2 Hybrid Nanoelectronics………………………………….. **8**

1.5 Carbon Nanotubes……………………………………………….... **9**

1.5.1 Single Walled Carbon Nanotubes (SWCNTs)…………... **10**

1.5.2 Multi Walled Carbon Nanotubes (MWCNTs)…………... **14**

1.6 Carbon Nanotube Field Effect Transistors (CNFETs)………… **15**

1.6.1 Types of CNFETs Based on Device Geometry………….. **18**

1.6.2 Prominent Advantages of CNFETs……………………… **20**

1.7 Organization of Thesis…………………………………………… **22**

2. Literature Survey……………………………………………………… **25**

2.1 Hybrid Circuits…………………………………………………... **25**

2.2 Hybrid Circuits with 3-D Integration………………………….. **27**

2.3 CNTs and CNFETs……………………………………………….. **29**

2.4 Spice Compatible Model for CNFETs………………………... **31**

2.5 Low Power Techniques……………………………………….. **33**

2.6 Summary…………………………………………………………. **38**

3. Hybrid CMOS-CNFET Voltage Controlled Oscillator…………... 41

3.1 Introduction…………………………………………………… **41**

3.2 Voltage Controlled Oscillators (VCOs) **41**

3.3 Hybrid CMOS-CNFET VCO………………………………….. **43**

3.4 Results and Discussion……………………………………….. **46**

3.5 Effect of CNFET Parameter Variation on VCO Frequency and Power Dissipation…………………………………………... **48**

3.6 Summary……………………………………………………….. **51**

4. Hybrid CMOS-CNFET OTA-C Filters……………………………. 53

4.1 Introduction…………………………………………………… **53**

4.2 Biomedical Filters……………………………………………... **53**

4.3 Hybrid CMOS-CNFET Transconductor………………………. **56**

4.4 Hybrid OTA-C Filters………………………………………….. **58**

4.5 Results and Discussions……………………………………….. **60**

4.6 Summary……………………………………………………….. **66**

5. Hybrid Voltage Reference Circuits………………………………… 67

5.1 Introduction…………………………………………………… **67**

5.2 Reference Voltage Sources…………………………………….. **67**

5.3 Hybrid Bandgap Reference utilizing CNFET Error Amplifier... **69**

5.4 Results and Discussion (Bandgap Reference)…………………. **74**

5.4.1 Power Supply Dependence (Line Sensitivity)…………… **74**

5.4.2 Temperature Dependence of the Bandgap Reference…… **75**

5.4.3 Power Supply Rejection Ratio (PSRR)………………….. **76**

5.4.4 Stability Analysis……………………………………….. **77**

5.5 Dual Threshold Voltage Reference Circuit……………………. **78**

5.6 Results and Discussions (Dual Threshold Voltage Reference)... **82**

5.7 Variability Analysis of the Voltage Reference…………………. **86**

5.7.1 Variability Issues in CNT and CNFETs…………………. **87**

5.7.2 Monte Carlo Analysis for the Effect of Diameter Variability on Voltage Reference………………………... **88**

5.7.3 Monte Carlo Analysis for the Effect of Inter CNT Pitch Variability on Voltage Reference………………………... **89**

5.8 Summary……………………………………………………….. **90**

6. Conclusion……………………………………………………………… 93

6.1 Introduction……………………………………………………. **93**

6.2 Summary of Results and Contributions………………………... **93**

6.3 Conclusions……………………………………………………. **96**

6.5 Future Work……………………………………………………. **97**

References……………………………………………………………… 99

Appendices

A Publications on Research Work…………………………………. **A-1**

B Analytical Expressions for Ballistic NCNFET………………….. **A-2**

C Key CNFET Model Parameters…………………………………. **A-3**

List of Figures

Figure 1.1	Scaling progression as the transistors are shrunk to the nanometer regime and the relative dimensions to indicate nanoelectronics era of the semiconductor industry…………………………………….	4
Figure 1.2	Classification of Extended/Beyond CMOS devices………………	6
Figure 1.3	Single-walled chiral type CNT construction from a 2-D graphene sheet by wrapping it up along the connection points. Zigzag and armchair CNTs shown separately……………………………...	10
Figure 1.4	MWCNT as a concentric arrangement of multiple (increasing diameter) SWCNTs……………..	14
Figure 1.5	CNFET Structure…………………………………………………	15
Figure 1.6	CNFET model based on ballistic theory…………………………..	16
Figure 1.7	Different structures/ types of CNFETs (a) CNFET with a bottom gate (b) CNFET with both top and bottom gate with electrostatically doped source-drain extension regions (c) CNFET with a top gate and chemically doped source-drain extension regions (d) CNFET with self-aligned top gate (e) CNFET with wrapped gate (f) CNFET with a gate beneath suspended CNT…...	19
Figure 1.8	Transport of carriers through a transistor channel (a) Unobstructed ballistic transport with channel lengths smaller than mean free path of carriers (b) Elastic scattering (c) Inelastic collisions with electrons losing energy………………………………………...	21
Figure 2.1	Heterogeneous 3-D integration for hybrid circuits………………..	27
Figure 2.2	Architecture of 3-D heterogeneous integration with efficient heat removal layers…………………………………………………….	29
Figure 2.3	CNFET model with parameters…………………………………..	32
Figure 2.4	(a) Clock gating and (b) Multi voltage technique…………………	34
Figure 2.5	Leakage mechanisms in aggressively scaled transistors………….	35
Figure 2.6	(a) Conventional power Gating (b) Hybrid power gating…………	36
Figure 2.7	(a) Stacking effect in a logic gate and (b) VTCMOS technique…...	37
Figure 2.8	(a) Forced transistor stacking and (b) Sleepy stack using parallel sleep transistors…………………………………………………...	37

Figure 3.1	(a) Tuning range, output frequency range and (b) linearity error in VCO……	43
Figure 3.2	Hybrid CMOS and CNFET VCO……	45
Figure 3.3	Output waveform of hybrid CMOS-CNFET VCO……	46
Figure 3.4	Frequency vs VCO control voltage for hybrid and CMOS VCOs...	47
Figure 3.5	Power dissipation vs VCO control voltage for hybrid and CMOS VCO……	48
Figure 3.6	Effect of number of tubes in CNFET on frequency and power dissipation for a hybrid VCO……	49
Figure 3.7	Effect of CNFET gate oxide thickness on VCO frequency and power dissipation for a hybrid VCO……	49
Figure 3.8	Effect of CNFET inter CNT pitch on VCO frequency and power dissipation for a hybrid VCO……	50
Figure 3.9	Effect of chiral vector (threshold voltage) on frequency and power dissipation for hybrid VCO……	51
Figure 4.1	Different types of filters with transition region between pass band and stop bands……	54
Figure 4.2	Hybrid transconductor……	57
Figure 4.3	Deep trenching in CMOS process for area efficient large capacitors……	59
Figure 4.4	1st order low pass OTA-C filter……	60
Figure 4.5	Frequency response of 1st order low pass OTA-C filter……	61
Figure 4.6	2nd order low pass OTA-C filter……	61
Figure 4.7	Frequency response of 2nd order low pass OTA-C filter……	62
Figure 4.8	Frequency response of OTA-C notch (50Hz) filter……	63
Figure 4.9	Frequency response of OTA-C high pass filter……	64
Figure 4.10	5th order elliptic low pass filter……	65
Figure 4.11	Frequency response of 5th order elliptic low pass filter……	65
Figure 5.1	Generating a current proportional to absolute temperature……	70
Figure 5.2	CMOS-CNFET hybrid bandgap reference……	72
Figure 5.3	CNFET based error amplifier used in bandgap reference circuit….	73
Figure 5.4	Reference voltage variation for V_{dd} sweep of 0V to 2.0V……	74

Figure 5.5 A close-up/magnified view for variation in reference voltage for V_{dd} between 1.2 V to 1.6 V………………………………………… 75
Figure 5.6 Temperature dependence of the circuit…………………………... 76
Figure 5.7 PSRR at 25°C and 75°C, V_{dd}=1.4V………………………………. 76
Figure 5.8 Stability / Transient analysis……………………………………... 77
Figure 5.9 A close-up of transient analysis…………………………………... 77
Figure 5.10 Threshold voltage as a function of chiral indices…………………. 80
Figure 5.11 A dual threshold CNFET voltage reference circuit………………. 81
Figure 5.12 Reference voltage and current as a function of V_{th} difference……. 83
Figure 5.13 Reference voltage and average power consumption as a function of V_{th} difference…………………………………………………….. 83
Figure 5.14 Reference voltage vs V_{dd} (Temperature sweep -25°C to 125°C)…. 84
Figure 5.15 PSRR at 25^{0}C , V_{dd} = 0.5 V………………………………………. 85
Figure 5.16 Transient analysis………………………………………………... 85
Figure 5.17 Imperfections in inter CNT pitch, diameter and mixed CNTs……. 87
Figure 5.18 Effect of diameter variability on reference voltage………………. 89
Figure 5.19 Effect of inter CNT pitch variability on reference voltage……….. 90

List of Tables

Table 3.1 A comparison of proposed VCO with conventional CMOS VCOs 48

Table 4.1 Performance comparison of filter structures…………………….. 66

Table 5.1 Performance comparison of bandgap reference w.r.t. performance metrics……………………………………………………………. 77

Table 5.2 Performance comparison with CMOS dual threshold voltage reference…………………………………………………………….. 86

LIST OF SYMBOLS

$a_{c\text{-}c}$	Nearest neighbor atomic distance between C-C atoms
$\vec{a}_1, \vec{a}_2$	Unit vectors
D_{CNT}	CNT diameter
φ_s	CNT surface potential
R_q	CNT quantum resistance
α	Optical phonon scattering constant
g_{CNT}	Transconductance of CNFET
a	Lattice constant
γ	C-C transfer energy constant
$V\pi$	Carbon π-π bond energy
e	Unit electron charge
k_B	Boltzmann constant
$\AA$	Angstrom
E_g	Bandgap
L_{ch}	Channel length
L_{ss}	Length of CNTs outside the top gate extended towards the source
L_{dd}	Length of CNTs outside the top gate extended towards the drain
W_g	CNFET gate width
W_{min}	Minimum gate width of CNFET
N	Number of CNTs
n, m	Chiral indices/ Chiral vector
$n1, n2$	Chiral indices/ Chiral vector
θ	Chiral angle
K_{gate}	Gate dielectric constant
T_{ox}	Gate oxide thickness
p^+	Heavily doped p-region
n^+	Heavily doped n-region
I_{ON}	On state current
I_{OFF}	Off state current
$I_{ON/OFF}$	On/Off current ratio
I_{out}	Output current

I_D	Drain current
I_{DS}	Drain to source current
I_{btbt}	Band to band tunneling current
C_L	Loading capacitance
C_{sub}	Gate-substrate coupling capacitance
Si	Silicon
Ge	Germanium
q	Elementary charge on electron
Cu	Copper
NO_2	Nitrogen dioxide
HfO_2	Hafnium oxide
Al_2O_3	Aluminum oxide
TaN	Tantalum Nitride
V_{DD}	Power supply voltage
V_{SS}	Ground
V_{out}	Output voltage
V_{in}	Input voltage
V_{SPH}	Higher switching point voltage
V_{SPL}	Lower switching point voltage
V_{hyst}	Hysteresis voltage
g_m	MOSFET transconductance
F	Clock frequency
f_{osc}	VCO oscillation frequency
f_{min}	Minimum frequency
f_{max}	Maximum frequency
f_c	Cut-off frequency
f_L	Lower cut-off frequency
f_H	Higher cut-off frequency
K_{vco}	VCO gain
Cox	Gate oxide capacitance

C_q	Quantum capacitance
Vth	Threshold voltage
V_{THN}	NMOS threshold voltage
V_{THP}	PMOS threshold voltage
V_T	Thermal voltage
V_{BE}	Base to emitter voltage of Bipolar Junction Transistor (BJT)
V_{GS}	Gate to source voltage
n	Diode ideality factor
I_s	Diode scale current
W/L	Width/Length (ratio) of transistor
TC_{eff}	Effective temperature coefficient
V_{dd_min}	Minimum supply voltage
V_{ref_max}	Maximum reference voltage
V_{ref_min}	Minimum reference voltage
V_{ref_nom}	Nominal reference voltage
ΔV_{dd}	Change in V_{dd}
P_{TAT}	Proportional to absolute temperature
T	Absolute temperature
σ	Standard deviation
μ	Mean
dB	Decibel

LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
BiCMOS	Bipolar Complementary Metal-oxide Semiconductor
BJT	Bipolar Junction Transistor
BTBT	Band-to-Band Tunneling
CLBs	Configurable Logic Blocks
CMOS	Complementary Metal Oxide Semiconductor
C-NEMS	Carbon Nanotube Nano-Electromechanical Switches
CNFET	Carbon Nanotube Field Effect Transistor
CNT	Carbon Nanotube
CSVCO	Current Starved Voltage Controlled Oscillator
Cu	Copper
CVD	Chemical Vapor Deposition
DAC	Digital to Analog Converter
DIBL	Drain-induced Barrier Lowering
ECG	Electrocardiogram
EEG	Electroencephalogram
EMG	Electromyogram
EOG	Electro-oculogram
FCC	Federal Communications Commissions
FinFET	Fin Field Effect Transistor
FPGA	Field Programmable Gate Array
GIDL	Gate-induced Drain Leakage
GNR	Graphene Nanoribbon
GNRFET	Graphene Nanoribbon Field Effect Transistor
HPCO	High Pressure Carbon Monoxide
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
III-V	Compound semiconductors obtained by combining group III and V elements in the periodic table

IoT	Internet of Things
IPD	Integrated Passive Device
IRDS	International Roadmap for Devices and Systems
LC	Inductor-Capacitor
LP	Low Power
LUT	Look up Table
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRAM	Magnetoresistive Random Access Memory
MTJ	Magnetic Tunnel Junction
MWCNT	Multi Walled Carbon Nanotube
NCNFET	n-type Carbon Nanotube Field Effect Transistor
Neg-C_g FET	Negative Gate Capacitance Field Effect Transistor
NW FET	Nanowire Field Effect Transistor
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCNFET	p-type Carbon Nanotube Field Effect Transistor
PLL	Phase Lock Loop
ppm	Parts per Million
PSRR	Power Supply Rejection Ratio
PTM	Predictive Technology Model
PVT	Process-Voltage-Temperature
PZT	Lead Zirconate Titanate
RC	Resistance-Capacitance
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuits
RFID	Radio Frequency Identification
RRAM	Resistive Random Access Memory
SCE	Short Channel Effect
SET	Single Electron Transistors
SiO_2	Silicon Dioxide
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	Subthreshold Swing/Slant

STT	Spin Transfer Torque
SWCNT	Single Walled Carbon Nanotube
TC	Temperature Coefficient
TFET	Tunnel Field Effect Transistors
TFT	Thin Film Transistors
ULP	Ultra Low Power
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
VTCMOS	Variable Threshold Voltage CMOS

Chapter 1

INTRODUCTION

1.1 Overview

The conventional CMOS scaling with respect to gate length, width, oxide thickness and supply voltage scaling will reach its limits because of increased static power consumption, short channel effects and variability. Increased static power dissipation, on account of excessive leakage in the ultra-scaled regime, has become a dominant concern and hence can't be disregarded for the special applications aimed to function in a tight power budget [1]. For applications, particularly involving portable devices, comprehensive efforts are required to curtail power consumption. For battery powered portable devices, reducing the power dissipation by means of meticulous design efforts so as to extend useful battery life becomes the prime objective. There is a particular class of emerging ultra-low power applications like wireless body area/sensor networks, Radio Frequency Identification (RFID), wearable and implantable biomedical devices [2]. These applications do not necessarily operate at higher speeds. The most important impetus for these applications is ultra-low power consumption to lengthen the battery life [1]–[3]. Another set of electronic systems that scavenge energy from the surrounding environment (light/heat), vibrations, human movements also do not have need of higher speeds but consume minuscule power [4]. For all such applications, one can opt for relaxed/ moderate speed and achieve significant benefits in terms of power consumption by means of specific efforts to curtail static power.

It is essential to explore different techniques to reduce power consumption to satisfy the need for ultra-low power circuits. Apart from architectural and circuit

level measures to reduce power consumption one has to pay attention to device level measures especially taking into account the benefits provided by emerging beyond CMOS and extended CMOS devices. These new class of devices having different kinds of structures and working principles provide enormous benefits in terms of aggressive scaling, particularly in sub 10nm regime. Examples of some of these devices include Carbon Nanotube Field Effect Transistors (CNFETs), Tunnel Field Effect Transistors (TFETs), Negative Capacitance FETs (Neg-C_g FETs), and Carbon Nanotube-based Nano-Electromechanical Switches (C-NEMS). These devices also offer significant avenues for potential hybrid nano-electronic circuits by co-integration with conventional CMOS devices. Devices listed above have gained significant attention due to their better subthreshold swing that can be achieved as compared to 60mV/decade limit posed by conventional CMOS. A steeper subthreshold swing implies improved On/Off ratios facilitating aggressive voltage scaling with reduced subthreshold leakage [5]. The most effective technique to reduce power consumption is to operate the devices in the subthreshold regime and to optimize the performance of the circuits for low power and moderate throughput applications. A lot of research has been carried out to investigate the performance of CMOS under subthreshold conditions. However, the use of hybrid technology is ignored by the research community. Therefore, it is necessary to investigate the performance of subthreshold circuits with hybrid technology.

Hybridization of CMOS with emerging nanotechnologies in a complementary manner plays an important role in reducing power consumption. This research work uses positive aspect of both CMOS and emerging nano-electronic device CNFET in a hybrid approach towards the design of ultra-low-power circuits. An ultra-low-power circuit with a hybrid approach with different (dual) threshold voltages for the

same technology is also investigated. Subsequent sections of this chapter present the motivation of the research, objectives of the thesis, the significance of hybrid nano-electronic circuits, details regarding carbon nanotubes, CNFETs and finally outline of the thesis is provided.

1.2 Motivation

A strong progress in nano-electronics will be the driving force of the world as well as the Indian economy. Advances in the field of nano-electronics are playing a vital role in the overall human development and will continue to do so in a longer time horizon. Nano-electronics will touch nearly every aspect of life: education, healthcare, entertainment, transportation, workplace and personal communication. As per International Roadmap for Devices and Systems (IRDS) future nano-electronic systems will sustain Moor's law by means of 3D monolithic heterogeneous integration. Carbon Nanotube Field Effect Transistors (CNFETs) are the promising devices for heterogeneous or hybrid integration with CMOS. This research work uses positive aspect of both CMOS and CNFET devices in a hybrid approach towards the design of ultra-low power circuits. By considering the significance of nano-electronics and its impact on overall human development there is a great necessity for further research in this area.

1.3 Objectives of Research

The objectives of this research work include-

- To study the significance of ultra-low power consumption for portable applications.
- To understand the existing techniques used to design ultra-low power circuits.
- To understand the challenges of ultra-low power circuit design.

- Propose the hybrid technology for ultra-low power circuits to cope up with design challenges at nano-scale.
- To design, simulate and analyze the proposed circuits.
- To compare proposed circuits with the existing circuits.

1.4 Nanoelectronics

Nanoelectronics refers to a multidisciplinary effort that shrinks critical dimensions of devices and interconnects to a nanoscale, ranging from less than a micrometer to one nanometer (just above atomic dimensions). The quest to continuously shrink device dimensions at extremities up to a few nanometers will endure to happen in the following decades in order to cater to ever-advancing technological applications for the benefit of mankind.

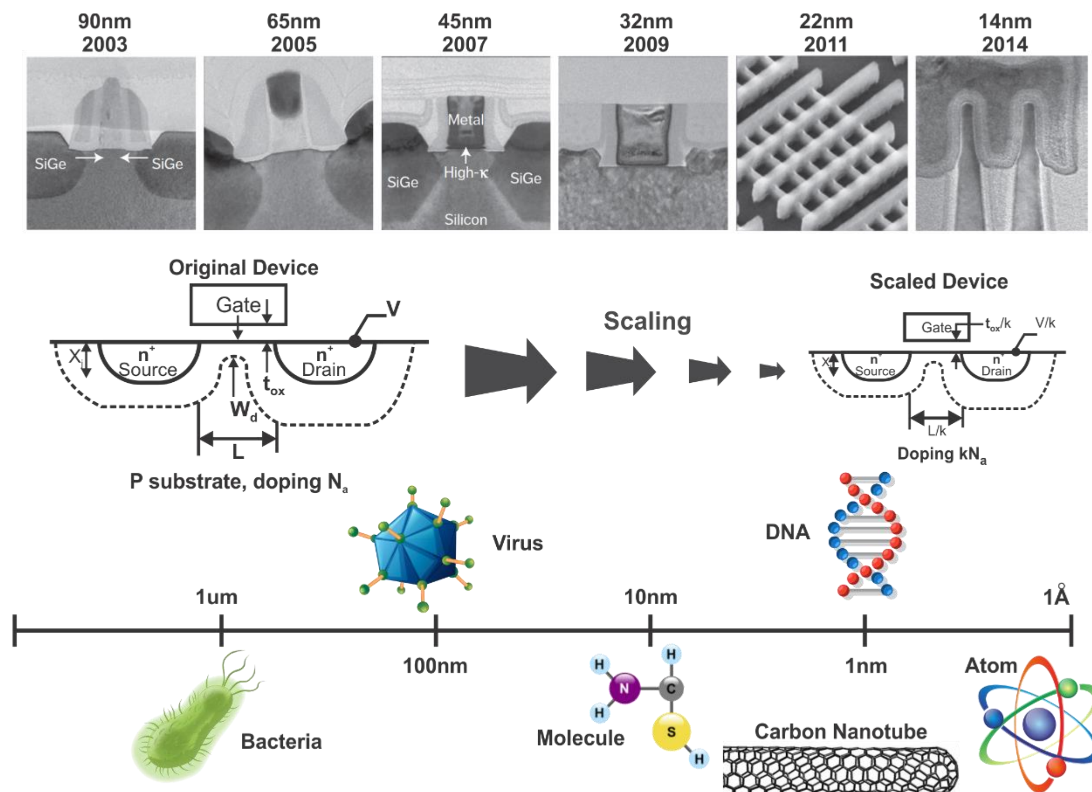


Fig. 1.1 Scaling progression as the transistors are shrunk to the nanometer regime and the relative dimensions to indicate nanoelectronics era of the semiconductor industry [6]

For the reason that the shrinking dimensions of the devices and interconnects happening continually and obeying Moor's law, we could state that the semiconductor industry is at present in a nanoelectronics era. In this nanoelectronics regime, due to devices being scaled down to extremities has resulted in the dominance of quantum phenomenon in semiconductor physics. Furthermore, scaling cannot happen indefinitely because transistors sizes cannot shrink smaller than atoms. The persistent scaling progression up to the nanometer regime and comparative dimensions with respect to bacteria, virus, molecule, DNA and atom is illustrated in Fig. 1.1. At present, technological hurdles in ultimately scaled planar MOS transistors have given the way for the development of new geometrically transformed nano-scaled FinFETs [6]. The last decade has witnessed innovations that introduced strained silicon in a 90nm technological node, high-K metal gates in the 45nm node (3.3 million transistors per mm^2). This was followed by the introduction of FinFETs in 22nm node (15.3 million transistors per mm^2) and 14nm node FinFETs (37.5 million transistors per mm^2) at the beginning of this decade. Currently, the semiconductor industry is witnessing the mass production of FinFET based 10nm node (100.8 million transistors per mm^2), with 7nm and 5nm nodes being in the development phase. This geometrically transformed FinFET technology offered distinctive advances in terms of greater electrostatic control over the channel that is encapsulated by a tall thin Si Fin, sharper subthreshold slant providing reduced off-state leakage and enhanced performance at ultra-low operating voltages [6]. However, to carry on the trend beyond this and to satisfy ultra-low voltage operations without unwarranted leakage in nanometer regime substantive efforts have been initiated to develop emerging devices to potentially replace MOS transistors referred as extended CMOS or Beyond CMOS devices [7]. Furthermore,

along with emerging devices, horizontal (planar) scaling will give a way to 3-D scaling by means of 3-D heterogeneous integration to sustain persistent scaling efforts.

1.4.1 Extended CMOS and Beyond CMOS Devices

There exist several contenders which will either possibly substitute CMOS transistors or might be used in concurrence with CMOS in a hybrid manner. Difficulty in further scaling of conventional CMOS devices has resulted in exploration of various emerging nano-electronic devices such as CNFETs, Tunnel FETs (TFETs), Single Electron Transistors (SET), Nanowire FETs (NW FET), Graphene Nanoribbon FET (GNRFET), Spin-FET, Negative gate capacitance FETs (Neg-C_g FETs), non-charge based spin wave devices, nanomagnetic logic and several others [7]. Based on their structure, working principle, potential to replace CMOS in future and their compatibility with CMOS fabrication these devices are referred as either Beyond CMOS devices or extended CMOS devices.

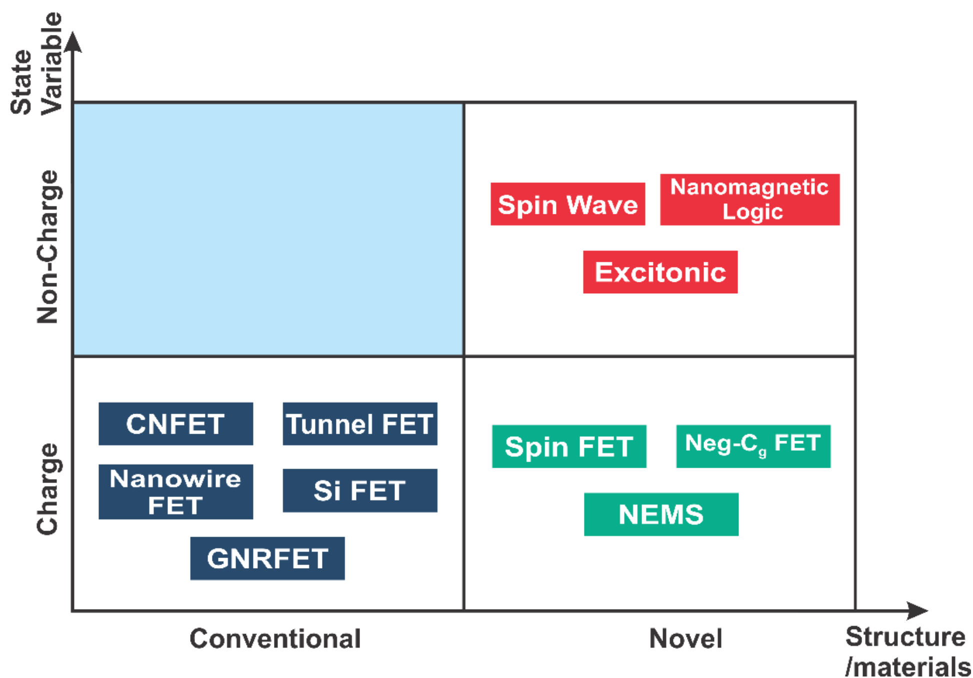


Fig. 1.2 Classification of Extended/Beyond CMOS devices [7]

Although the terms extended CMOS and beyond CMOS are used interchangeably, as per "International Roadmap for Devices and Systems" (IRDS), 2017 Edition, the bifurcation as shown in Fig. 1.2 is based on the novelty of materials and/or structures and based on whether logic processing is a charge based (electrons) or non-charge based [7]. The non-charge based devices typically rely on ferromagnetic, spintronics principles utilizing novel materials and/or structures. Amongst these devices, the TFET devices with very low on state current and ultra-low voltage levels are favorable options for ultra-low-power applications [8]. TFETs with different structures, working on tunneling mechanisms, have shown subthreshold slant lesser than 60mV/dec. but at the expense of poor performance. Nanowire FETs exhibiting reduced short channel effects, near ballistic conduction, consists of a nanowire channel made from semiconductors such as Si, Ge, III-V materials [9]. GNRFETs with graphene nanoribbon as a channel material also hold encouraging potential but still lag in overall operation as compared to their CNT counterparts (CNFETs) [10]. Negative C_g FETs replace conventional gate dielectrics by a ferroelectric material such as Lead Zirconate Titanate as a negative capacitance to obtain lesser than 60mV/dec. subthreshold slants enabling low power operation [11]. Another set of futuristic devices include spin-FETs, spin-MOSFETs, pseudo-spin-MOSFETs and several others which work on the principle of spin manipulation in a semiconductor channel inserted between ferromagnetic source-drain regions [7]. NEM switches are basically nano-scaled mechanical switches which can be turned on and off electrostatically, are excellent candidates as power gating switches (because of zero leakage currents) and for moderate speed low power computing [12]. Apart from these charge-based devices, there exists a lot of interest in totally different (non-charge based, non-compatible with CMOS) logic processing devices

such as spin wave devices (utilizing spin wave oscillations), nanomagnetic logic (utilizing fringing field interactions amid magnetic islands) and excitonic transistors(utilizing excitons instead of electrons) [7]. However, on a longer horizon, it seems that CNFETs on account of better performance and power efficiency will eventually be capped as the ultimate transistor. This research work has focused on utilizing CNFETs along with CMOS in a hybrid manner and hence CNFETs are discussed separately in the subsequent sections.

1.4.2 Hybrid Nano-electronics

One of the approaches for effective utilization of these extended CMOS or Beyond CMOS devices is to have diverse hybrid circuits such as hybrid CMOS-CNFET, CMOS-SET [13], CMOS-MTJ [14], CMOS-Memristor [15], and CMOS-TFET [16]. Hybrid realization of electronic circuits utilizing conventional MOSFETs and emergent nano-electronic devices has been presented by several researchers. These hybrid circuits further lead to the 3-D heterogeneous integration of CMOS with these emerging devices. Hybrid realization of digital logic, memory, analog circuits, biosensor interfaces and interconnects are the possibilities with this kind of approach. These hybrid circuits will provide a means to sustain Moors law, extend CMOS functionality and satisfy stringent power budgets of portable electronic systems by 3-D heterogeneous integration. Both circuit level as well as architecture level hybrid approach can be used in a complementary manner. In a circuit level approach, the circuit may consist of at least two different kinds of devices. Architectural level hybridization may involve different circuit blocks using different devices.

Though extended CMOS or devices beyond CMOS such as CNFETs are proposed as an alternative to CMOS by the different researchers, but in near

prospect, it is very difficult to substitute the CMOS technology because of research progression and commercial impact of CMOS based devices. The CNFET technology can be combined with cost effective and reliable CMOS technology. The resulting hybrid CMOS-CNFET circuits can form the basis of a variety of circuits and systems. Several analog/digital electronic circuits and systems can be designed with the hybrid approach to take advantage of superior properties of CNFETs while building the hybrid circuits on the top of existing CMOS technology.

The proposed research used SPICE models and simulations to investigate circuits using a hybrid implementation of CMOS and CNFETs. Spice simulations of proposed circuits were performed. Hybrid approach for the circuits involving different threshold voltages of the devices of the same technology was also investigated. Following circuits were investigated in a hybrid approach.

i. Hybrid CMOS-CNFET Voltage Controlled Oscillator(VCO)
ii. Hybrid CMOS-CNFET OTA-C filters
iii. Hybrid Bandgap reference circuit
iv. Dual threshold two transistor voltage reference circuit

1.5 Carbon Nanotubes

The carbon nanotubes are cylindrical shaped nanostructures made from rolled graphene sheets (an allotrope of carbon) that exist in two forms:

(i) Single-walled carbon nanotube (SWCNT) and
(ii) Multi-walled carbon nanotube (MWCNT).

A promising new material in a multi-walled form was reported by Iijima in 1991 [17]. Further, in 1993 Iijima reported a single-walled form [18]. Since the discovery of the carbon nanotubes, enormous interest has been created in the field of nanoscience, technology and diverse applications of nanotubes.

1.5.1 Single-Walled Carbon Nanotubes (SWCNTs)

A single-walled CNT (SWCNT) as shown in Fig. 1.3 can be envisaged as a pane of graphite, which is rolled up and linked together along a roll- up vector drawn within six carbon rings [19].

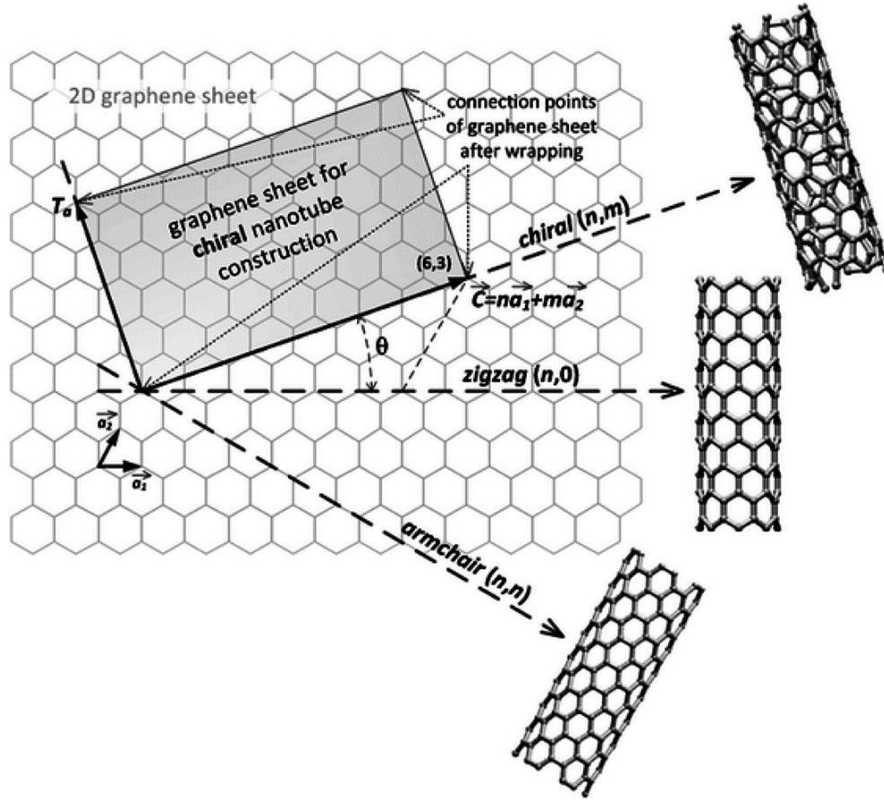


Fig. 1.3 Single-walled chiral type CNT construction from a 2-D graphene sheet by wrapping it up along the connection points. Zigzag and armchair CNTs shown separately [19]

The roll-up vector is also called as a chiral vector. The angle formed between the horizontal axis and the roll-up vector is called as chiral angle denoted by symbol θ expressed as,

$$\theta = \cos^{-1}\frac{2n+m}{2\sqrt{n^2+nm+m^2}} \tag{1.1}$$

An SWCNT can be classified as either metallic without a bandgap or a semiconductor with a certain bandgap, dependent on the angle θ of the atomic arrangement with respect to the tube axis[20]. The angle θ is the function of indices

(n, m). By referring the index (n, m) shown in Fig. 1.3, the nanotube is metallic in nature, if n = m or n-m = 3i where i is an integer (nonzero). Or else, the tube is semiconducting. The chiral vector $\vec{C} = n\vec{a}_1 + m\vec{a}_2$ is made up of chiral indices n, m with respective unit vectors $\vec{a}_1$ *and* $\vec{a}_2$. $\vec{a}_1$ is a unit vector comprising two adjacent segments of the hexagon along the horizontal axis of the honeycomb structure. Similarly, $\vec{a}_2$ is a unit vector comprising two adjacent segments of the hexagon along the vertical axis of the honeycomb structure. As an illustration, Fig. 1.3 shows the chiral vector with indices n=6 and m=3 around which the graphene sheet can be rolled up at appropriate connection points to make a CNT. The length of the line segments perpendicular to both the ends of the chiral vector decides the diameter of the CNT. This kind of rolled up sheet with a chiral angle between 0° to 30° is called as a chiral type of CNT. Similarly, a CNT with a chiral vector (n, 0) is referred as zigzag type while a CNT with a chiral vector (n, n) is called armchair type[19], [20]. CNTs can take sizes (diameters) ranging from ~0.4nm to 3nm. The indices n and m also decide the diameter and hence significant properties of the CNTs. The CNT diameter in terms of indices n and m is given by an expression,

$$D_{CNT} = \frac{a\sqrt{n^2 + n.m + m^2}}{\pi} \tag{1.2}$$

The diameter expression (equation 1.2) is applicable to all the three types ie. Chiral, armchair and zigzag nanotubes. The expression for armchair and zigzag diameters respectively can be simplified as,

$$D_{CNT} = \frac{a\, n\sqrt{3}}{\pi} \tag{1.3}$$

$$D_{CNT} = \frac{a\, n}{\pi} \tag{1.4}$$

The term in the diameter expression $|\vec{a}_1| = |\vec{a}_2| = a = 0.246nm$ (2.46Å) is the magnitude of unit vectors which is the lattice constant of graphene. It can be seen from the diameter expression that a same diameter tube is possible with different chiral indices. As an illustration, a diameter of 1.49nm results with indices (19, 0) and (16, 5). A diameter of the order of few nanometers and significantly larger lengths of the tubes gives an aspect ratio that is considerably larger than any other material. The CNT diameter is an imperative parameter deciding the bandgap and hence the threshold voltage of Carbon Nanotube Field Effect Transistor (CNFET). The bandgap of a single walled semiconducting nanotube is related to the diameter by an expression,

$$E_g \approx \frac{2\,\gamma\, a_{c-c}}{D_{CNT}} \tag{1.5}$$

$$E_g \approx \frac{0.8890eV}{D_{CNT}} \tag{1.6}$$

Where γ = 3.13eV is C-C transfer energy constant and $a_{c\text{-}c} = \frac{a}{\sqrt{3}}$ = 0.142nm is the nearest neighbor atomic distance between C-C atoms. Metallic tubes with n=m (armchair) or the tubes satisfying n-m = 3i have no bandgap. For semiconducting nanotubes, the bandgap would decrease with an increase in CNT diameter. The bandgap expression also implies that different chiral indices giving same diameters also possess the same bandgap.

CNTs reveal outstanding thermal and mechanical characteristics, possessing a thermal conductivity of the order of ~3000W/m-K, Young’s Modulus of ~1TPa [21]indicating very strong material (stronger than diamond) and high elastic stiffness (~5-10 times stiffer than steel).

CNTs with their unique properties are finding numerous present and futuristic applications[22]–[24]. First and foremost, CNT applications include

microelectronics wherein CNTs form the basis for Field Effect Transistors (CNFETs), CNT thin-film transistors (TFTs), flexible electronics, CNT interconnects, electrodes, CNT nano-electromechanical switches (CNEMS) and heat sink materials[22], [25] The semiconducting CNT array constitute the channel of CNFET. CNFET structure, benefits and other aspects of CNFETs are discussed in Section 1.6.2. Metallic CNTs are also finding applicability in nanoscale VLSI interconnects due to superior thermal and electrical properties than traditional Cu interconnects such as low resistivity, high current carrying capacities and electro-migration immunity[26]. In an era of ultra-scaled semiconductor chips, we also need faster and denser interconnects but with scaled and dense interconnects resistivity increases while capacitance increases. Bundled metallic CNT interconnects provide a new opportunity to improve energy-delay benefits for the future ultra-scaled semiconductor chips.

Apart from microelectronics CNTs offer numerous other applications involving diverse fields such as environment, energy, material science, healthcare and biotechnology[22]. Environmental applications of CNTs include water purification membranes, sensing chemical vapors, cleaning oil spills using CNT sponges. CNTs also find applications in battery technology, fuel cell catalysts, CNT-Si heterojunctions in photovoltaic technology and supercapacitors. CNTs have found widespread interest in biotechnology and healthcare applications such as biosensors detecting protein, NO_2 in bloodstream, surface coatings for dental implants and low-impedance neural interface electrodes[22], [24] Besides this CNTs have been used in different kinds of composite materials to modify their mechanical properties, coating and films that alter the surface properties of metals and alloys. Besides all these interesting and diverse applications of CNTs, its worth to mention that a few

amongst them are commercialized or incorporated into products but many of these applications are still in experimental or prototyping phase due to several difficulties in CNT synthesis and processing requirements of individual applications.

1.5.2 Multi-Walled Carbon Nanotubes (MWCNTs)

MWCNT appear like a concentric arrangement of multiple SWCNTs, but with striking differences. The diameter of MWCNT ranges from 5-50 nm depending upon the number of concentric SWNTs and the interlayer spacing is of the order of 3.4Å. Fig. 1.4 gives an idea about MWCNT as a concentric arrangement of multiple (increasing diameter) SWCNTs.

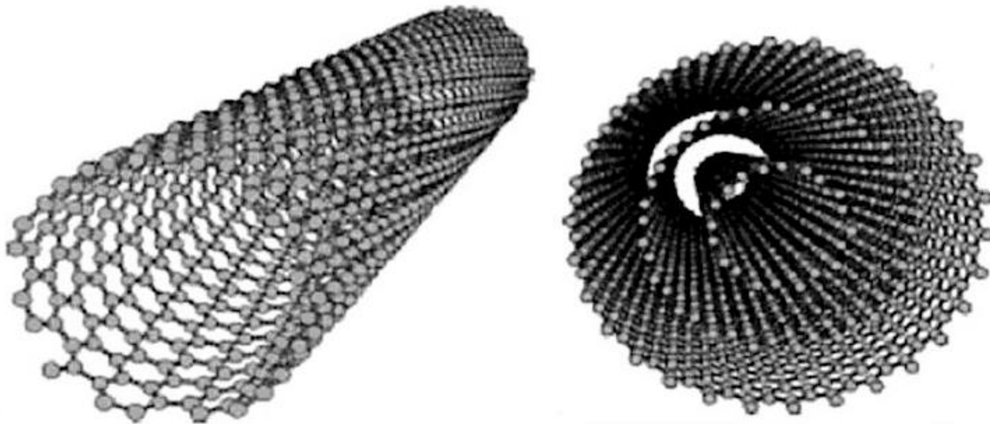


Fig. 1.4 MWCNT as a concentric arrangement of multiple (increasing diameter) SWCNTs

They are easy to produce in large quantity with lengths 100 times larger than their diameters, possess high electrical conductivity, tensile strength, thermal and chemical stability [27]. MWCNTs are one of the advanced engineering materials having diverse applications in the fields of material science, space technology, biological sciences, sensors, composites and polymers etc. However, its structural arrangement is intricate and the physical defectiveness may diminish their distinctive properties. MWCNTs can be incorporated into high-density interconnects to satisfy emergent needs such as reduced delay, high performance, higher current densities, electromigration, a decrease in physical spacing, reducing power

consumption and parasitic effects [28]–[30]. It can be seen that the MWCNT interconnect delay is diminutive than that of copper interconnects and this enhancement is more evident for longer interconnect lengths [29]. This shows MWCNT can bring substantial improvement in overall circuit performance in futuristic VLSI interconnects.

1.6 Carbon Nanotube Field Effect Transistors (CNFETs)

Progress made in recent year's shows that the limitations of traditional CMOS such as the exponential increase of leakage currents in scaled transistors can be overcome to some extent, and further scaling of device sizes is possible with CNFET technology. In the sub-10nm regime of the scaled devices, CNFETs outperform potential alternatives of the conventional MOSFET. Therefore, there exist huge opportunities for the integration of CNFETs into circuits and systems for the futuristic electronic applications. CNFETs, owing to very high electron mobility, efficient transport of carriers and improved gate electrostatics carbon nanotubes serve as an excellent active channel of a transistor device. Due to very small diameters of the CNTs, the CNT channel exhibit very large aspect ratio (Length/Diameter). The CNFET structure is shown in Fig. 1.5.

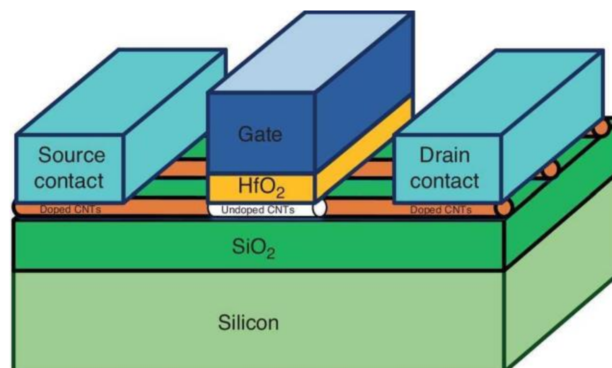


Fig. 1.5 CNFET Structure

CNTFETs are the FETs that make use of semiconducting CNTs as channel material between two metal electrodes that act as source and drain contacts. Silicon

still provides the substrate, mechanical support and heat transport mechanism for the hybrid device structure of the resulting CNFET. As shown in Fig. 1.5, this three terminal device consists of the SWCNT array, acting as a conducting channel, bridging the source and drain contacts. Individual CNT placed between source-drain contacts consists of un-doped (intrinsic) region forming the channel and doped CNT region. The operation principle of CNTFET is similar to that of traditional silicon devices. The device is turned on or off electro-statically via the gate. For channel lengths shorter than the mean free path of charge carriers, CNFETs are considered to obey ballistic transport theory [31] which can be used to analytically determine various fundamental metrics of CNFETs such as drain current(I_D), on state current, threshold voltage(V_{th}), transconductance(g_m) and subthreshold current. The CNFET modeled as per ballistic theory is depicted in Fig. 1.6 [31].

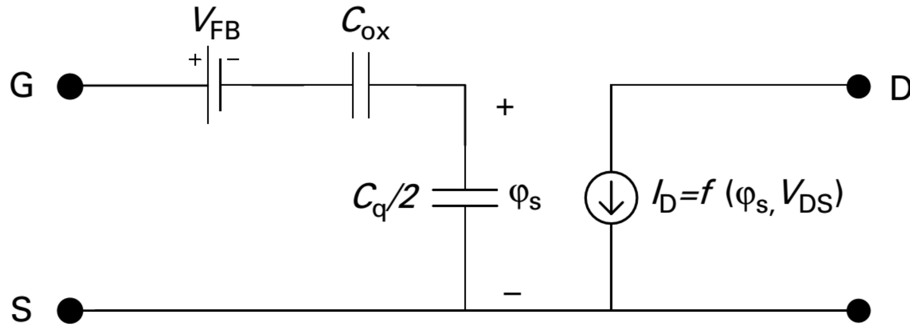


Fig. 1.6 CNFET model based on ballistic theory [31]

Considering optical phonon scattering, the expressions of I_D [31] for a ballistic NCNFET and PCNFET are given by equation 1.7 and equation 1.8 respectively,

$$I_D = \frac{k_B T}{e.R_q}\{ln[1 + e^{(2e\varphi_s - E_g)/2k_B T}] - ln[1 + e^{(2e\varphi_s - 2e\alpha V_D - E_g)/2k_B T}]\} \quad (1.7)$$

$$I_D = \frac{k_B T}{e.R_q}\{ln[1 + e^{(-2e\varphi_s - E_g)/2k_B T}] - ln[1 + e^{(-2e\varphi_s + 2e\alpha V_D - E_g)/2k_B T}]\} \quad (1.8)$$

In these expressions for I_D, k_B is the Boltzmann constant, e is unit electron charge, T is the temperature, R_q the quantum resistance, φ_s is the surface potential, α the optical phonon scattering constant and E_g is the bandgap. The expressions for

NCNFET are also listed in Appendix B. The parameter α=1 corresponds to ballistic transport and α<1 corresponds to partial ballistic transport in the CNTFET channel. In a nutshell, we can say, $I_D = f(\varphi_s, V_D)$. The φ_s of CNT (for a top-gated CNFET like the one shown in Fig.1.5) is a function of gate oxide capacitance (C_{ox}), the quantum capacitance (C_q) and the gate drive (V_{GS}). The gate drive electrostatically controls the amount of φ_s which in turn alters the charge density [31]. The drain current equations 1.7 and 1.8 consider positive φ_s for NCNFET and negative φ_s for PCNFET. The equation 1.7 can be recast to obtain the approximated ON current expression [31] for NCNFET (corresponding to active region with V_{GS} exceeding V_{TH} and drain voltage exceeding (V_{GS} - V_{TH})).

$$I_{ON} \approx \frac{k_B T}{e.R_q} ln\left[1 + e^{(2e\varphi_s - E_g)/2k_B T}\right] \tag{1.9}$$

CNFET is the utmost favorable technology to extend or supplement modern CMOS technology due to various reasons: First, the working principle and the device geometry are similar to CMOS devices; we can reuse the existing CMOS design infrastructure. Second, we can reuse the CMOS fabrication process. And the most important reason is that CNFET has the best experimentally demonstrated device current carrying ability.

The physical arrangement of CNTs in the CNFET device structure decides important aspects of CNFETs such as its channel length (L_{ch}), gate width (W_g), inter CNT pitch and number of CNTs. The length of the intrinsic CNT region beneath the gate is the channel length. The gate width approximated by an equation 1.10, depends upon the minimum gate width (W_{min}), number of CNTs (N), the diameter of individual CNT and the inter CNT pitch.

$$W_g \approx Max(W_{min}, (N-1).Pitch + D_{CNT}) \tag{1.10}$$

The number of CNTs and the inter CNT pitch are the important factors deciding the drain current in CNFETs. For a fixed width device increasing CNT count (ie. decreasing the pitch) increases the current until CNTs do not come too close and charge screening plays a reverse effect of decreasing the current.

1.6.1 Types of CNFETs Based on Device Geometry

There exist different geometrical structures [31]–[33] (Fig. 1.7) to realize a CNFET viz.

(i) CNFET with a bottom gate

(ii) CNFET with both top and bottom gate with electrostatically doped source-drain extension regions

(iii) CNFET with a top gate and chemically doped source-drain extension regions

(iv) CNFET with a self-aligned top gate

(v) CNFET with wrapped gate

(vi) CNFET with a gate beneath suspended CNT.

The CNFETs with bottom gate approach [31] exhibits very poor gate control over the channel (in a low voltage regime) on account of quite a thick gate dielectric. This imposed a difficulty in turning the device ON at low voltage levels. The bottom gate approach lacks the feature of controlling the gate of an individual transistor in case of multiple CNFETs. Furthermore, the Schottky barrier is formed in this type of device geometry at the drain-source and metal interfaces giving rise to considerable contact resistance [34]. The CNFET structure with both top and bottom gate shown in Fig. 1.7(b) uses electrostatically doped source-drain extension regions with the help of the bottom gate [31].

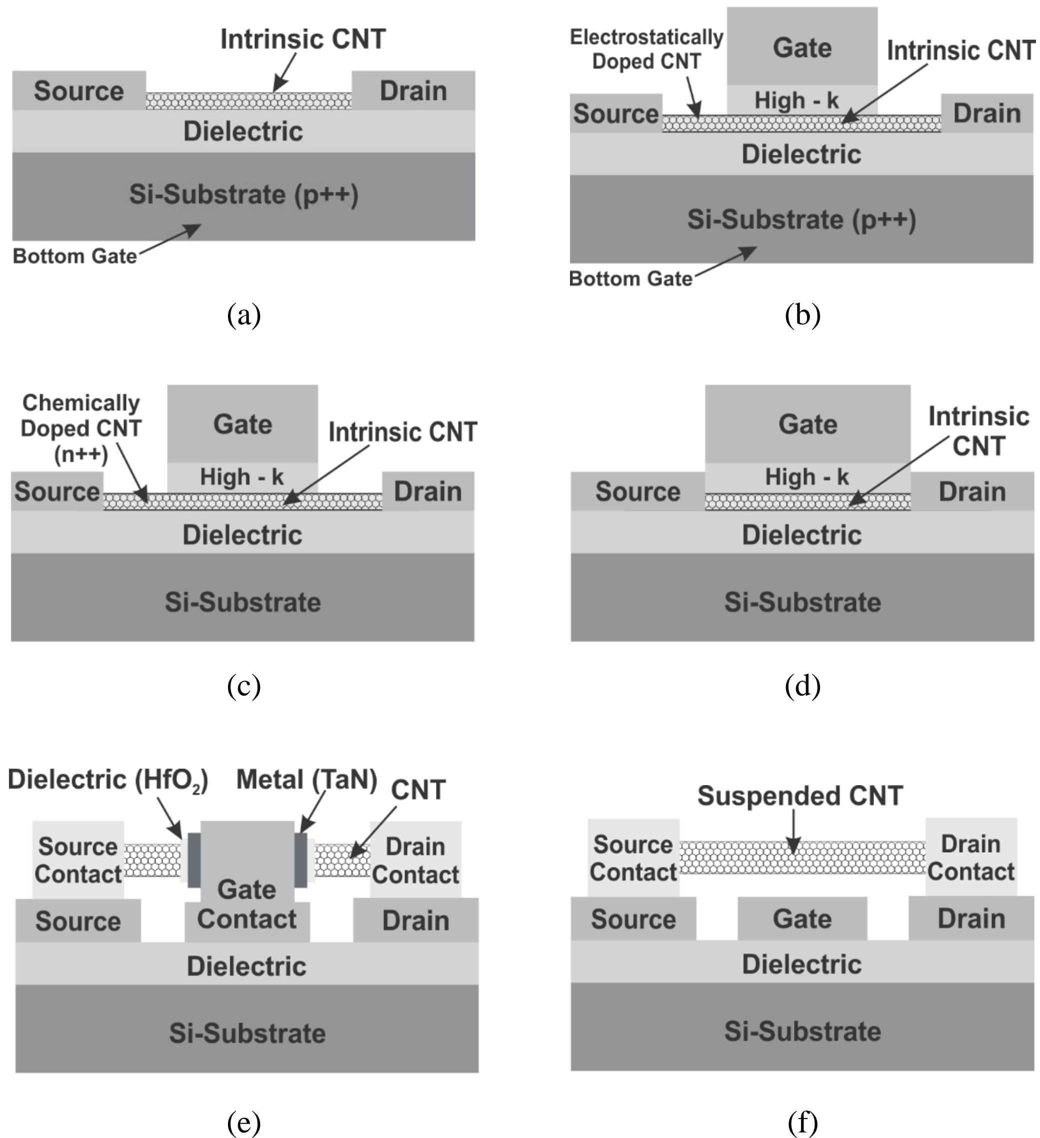


Fig. 1.7 Different structures/ types of CNFETs (a) Bottom gate CNFET (b) CNFET with both top and bottom gate with electrostatically doped source-drain extension regions (c) CNFET with a top gate and chemically doped source-drain extension regions (d) CNFET with self-aligned top gate (e) CNFET with wrapped gate (f) CNFET with a gate beneath suspended CNT [31]–[33]

Later on, significant improvement was done in a CNFET with a top gate geometry with chemically doped source-drain extension regions, also called as MOSFET like CNFET owing to its geometrical similarity with Si MOSFET. Top gate CNFET with chemically doped source-drain extension regions is the most common device geometry being used amongst the other structures. This research work uses MOSFET like top gated CNFETs for the design of different hybrid

CMOS-CNFET circuits. Top gate structure offered superior performance in terms of improved drive current, better electrostatic control, higher transconductance per CNT and scalable device geometry. A native oxide formed during the manufacturing process enables the realization of top gate self-aligned CNFETs without source-drain extension regions [31]. In a CNFET with wrapped gate, electrostatic control of channel can further be improved by imbibing a geometry that completely surrounds the nanotubes by HfO_2 / Al_2O_3 gate dielectrics and Tantalum Nitride (TaN) metal gate [32]. This type of device structure brings benefits on two fronts, first, the best possible gate control and second, the charge screening in a closely placed neighboring CNTs is reduced because of the wrapped gate of each and every CNT. However, these benefits are not much significant and top gated CNFETs, therefore, offer better overall performance. Another device structure uses suspended CNTs between source-drain regions with a physical separation from substrate and dielectric. This type of CNFET structure results in reduced hysteresis, a better subthreshold slope with ambipolar behavior [33].

1.6.2 Prominent Advantages of CNFETs

CNFETs have found widespread interest due to many of its excellent properties and offer distinct advantages over Si MOSFETs. The prominent advantages of CNFETs include the high current density, high electron mobility, better control over channel formation, reasonable energy gap, near ballistic transport of charge carriers, high performance at low operating voltages and scalability below 10nm with minimal short channel effects [35], [36]. In spite of several technological challenges associated with fabrication of CNFETs, encouraging results have been reported so far by successfully realizing CNFETs with high carrier mobility (1600 cm^2/V-s), current density (150μA/μm), $I_{ON/OFF}$ (10^4) and transconductance, g_m (80μS/μm) [37].

Better control over channel formation results due to one-dimensional nature of ultrathin CNT channel as compared to three-dimensional geometry offered by bulk MOSFET.CNFETs, owing to unique one-dimensional CNTs forming the channel, support nearly ballistic transport of charge carriers. This is evident from the fact that in the aggressively scaled devices channel lengths would be smaller than the mean free path of the charge carriers. This means electrons can travel in an unobstructed manner maintaining their momentum as well as their phase. Contrary to this bulk Si MOSFETs experience different scattering mechanisms resulting in mobility degradation and a noticeable decrease in channel current. Electrostatically acquired energy by the charge carriers, under the influence of voltages applied at device terminals, is partially lost due to such type of diffusive and scattered transport. Different transport mechanisms of charge carriers are shown in Fig. 1.7.

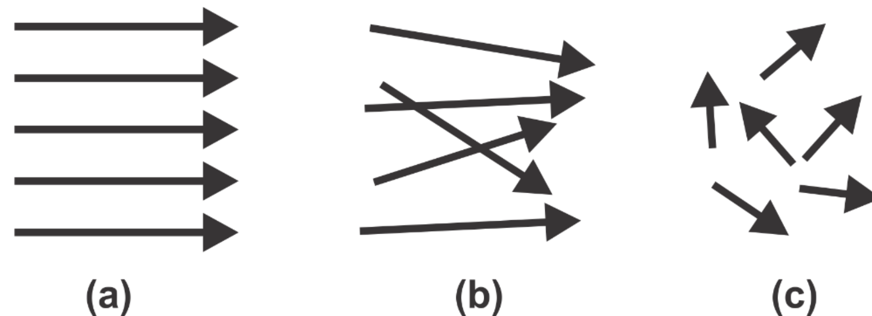


Fig. 1.8 Transport of carriers through a transistor channel (a) Unobstructed ballistic transport with channel lengths smaller than mean free path of carriers (b) Elastic scattering (c) Inelastic collisions with electrons losing energy

CNFETs obviously outperform Si MOSFETs with respect to near ideal transport of carriers in the channel. However, difficulty in realizing ideal ohmic contact between the metal-CNT interface, a finite channel resistance due to manufacturing defects and the scattering thereof contributes in a non-ideal transport of carriers in CNFETs. The fabricated CNFETs are certainly not immune from defects and hence introduce various kinds of scattering effects including elastic scattering, inelastic

scattering (optical phonon scattering and acoustic phonon scattering) [38]. Based on the nature of metal-CNT contact, carrier transport in CNFETs can be ballistic (ohmic/Schottky) for channel lengths shorter than mean free path and diffusive (ohmic/Schottky) for channel lengths larger than mean free path. Apart from simple integrated circuits such as logic gates and ring oscillator, CNFETs have been extensively investigated for many analog and radio frequency (RF) circuits. Recent reports have shown that CNFETs are potentially promising candidates for highly linear RF circuits and applications. Researchers in [39] have demonstrated that CNFETs possesses linearity that is comparable to that of conventional MOSFETs.

Despite the promising progress of CNFETs, there remain challenges such as the high fabrication cost of CNFETs and manufacturing issues concerning mixed semiconducting-metallic CNTs, impurities in synthesis process and variability.

1.7 Organization of Thesis

The thesis is arranged in six chapters describing the context, aims, objectives of the research, motivation, literature review, methods and techniques employed and the research contributions.

Chapter 1: Introduction: briefly describes the importance of low power circuits and their applications to wearable, implantable and portable electronic systems. Scaling limitations of conventional CMOS devices and the importance of hybrid circuits are explained in the context of the proposed research. The ongoing progress in the field of nanoelectronics and emergence of novel extended/beyond CMOS devices is covered in this chapter. A brief introduction of Carbon Nanotubes, CNFETs, and their applications are also described. The chapter explains the motivation of the study, enlists the objectives of the research and concludes by providing an outline of the thesis.

Chapter 2: Literature Survey: This chapter highlights development of techniques and technologies for the low power circuits. The literature review of existing hybrid CMOS-CNFET circuits and hybrid circuits with 3D integration is covered. A review of the development of carbon nanotubes, CNFETs and Stanford model for CNFETs is also described. Limitations, shortcomings of existing techniques are presented.

Chapter 3: Hybrid CMOS-CNFET Voltage Controlled Oscillator (VCO): This chapter describes the development of hybrid VCO, analysis, experimental work and the results obtained.

Chapter 4: Hybrid CMOS-CNFET gm-C Filters: Description of biomedical filters, the significance of electronic filters, proposed hybrid filter structures, experimental evaluation and results are presented in this chapter. Applications of hybrid gm-C filters to biomedical signal processing are also discussed in this chapter.

Chapter 5: Hybrid voltage reference circuits: The hybrid realization of proposed bandgap reference circuit and a dual threshold voltage reference circuit are presented and discussed in this chapter. Variability analysis in the presence of different imperfections in CNFETs for the hybrid dual threshold voltage reference is also covered.

Chapter 6: Conclusion: This chapter provides a summary of the investigations, conclusions drawn from the results, and suggestions for further work.

Chapter 2

LITERATURE SURVEY

After a thorough study of the existing literature, we have provided a literature review comprising methods, techniques and a summary of contributions by various researchers in the context of hybrid circuits, systems, emerging nano-electronic device (CNFETs), and low power research. The literature review covers-

- Hybrid circuits
- Hybrid circuits with 3-D integration
- CNTs and CNFETs
- Spice compatible model for CNFETs
- Low power techniques

2.1 Hybrid Circuits

Hybrid nano-electronic circuits quickly drew attention after the introduction of various extended CMOS devices like CNFETs. Variety of hybrid circuits such as a simple inverter, a cascode amplifier, a power gating scheme for sleep mode power reduction, hybrid FPGAs, and quite a complex hybrid/heterogeneously integrated 3-D circuits have been reported so far. Meric et.al. proposed a hybrid technology and demonstrated the integration of CMOS and CNFET device for a simple hybrid CMOS-CNFET inverter[40]. The hybrid co-integration was done as a post process after a conventional CMOS fabrication. A complex fabrication process involved chemical vapor deposition (CVD) and photolithography steps to obtain a single hybrid inverter. Usmani et al. presented performance optimization of a hybrid CMOS-CNFET inverting amplifier and compared the proposed hybrid circuit performance with that of a conventional CMOS inverting amplifier [41].

Performance of the same circuit using CMOS, CNFET and hybrid CMOS-CNFET approach was compared. Optimized parameters such as inter CNT pitch, CNT diameter and number of tubes were estimated. Authors showed performance improvement in terms of gain, bandwidth, slew rate and output resistance. Akinwande et al. proposed the first RF circuit with nMOS-pCNFET co-integration for a cascode amplifier. The fabrication process employed was a room temperature dielectrophoresis for integrating CNTs on the prefabricated silicon chip. The major benefit of the fabrication technique used is a complete decoupling of CNT and CMOS processing. A hybrid cascode configuration is obtained by utilizing both CMOS and CNFET on the same chip [42]. Cho et al. demonstrated the application of CNT-CMOS hybrid system for chemical sensing application by using the property of variation in conductance of CNT upon exposure with certain gases and chemicals [43]. Kim et al. investigated a power gating scheme with CNFETs as sleep transistors for a conventional CMOS logic cell. Replacement of CMOS sleep transistors by CNFETs for power gating is proposed by the authors. Just like MOSFET sleep transistor design, considerable efforts are required to find optimized CNFET parameters to satisfy design goals in ultra-low power regime. Authors proposed a ring styled, multi-mode and 2-pass hybrid power gating structures. The hybrid scheme achieved reduced sleep mode leakage power consumption, delay, rush current, and area however at the cost of little increase in wakeup time [44]. FPGA architectures can also be altered to include both CMOS and CNFET devices in a complementary manner so as to reap significant benefits in terms of area, power efficiency and performance. Moaiyeri et al. presented a hybrid FPGA utilizing CNFETs as routing switches while maintaining the rest of the FPGA architecture as it is [45]. The configurable logic blocks (CLBs) and SRAMs were implemented

using CMOS technology. Authors reported average power dissipation reduction by up to 6%, performance gain by about 30%, lesser susceptibility to PVT variations and considerable leakage power reduction. Zhou et al. proposed a hybrid FPGA design using carbon nanotube-based nano-electromechanical (NEM) switches as a replacement for SRAM cells in lookup tables (LUTs) [46]. Chakraborty et al. presented a leakage control scheme utilizing a CNT-based nano-electromechanical switch for conventional CMOS logic and memory circuits[47].

2.2 Hybrid Circuits with 3-D Integration

Shulaker, et al have demonstrated the capabilities to fabricate the chip that comprises 3-D integrated hybrid circuits using a process that is compatible with existing silicon fabrication technology [48]. Heterogeneous integration as depicted in Fig. 2.1, comprising CNFET gas sensors and logic, data storage (RRAM), CMOS and CNFET logic were achieved with the dense vertical interconnects on a 3-D chip.

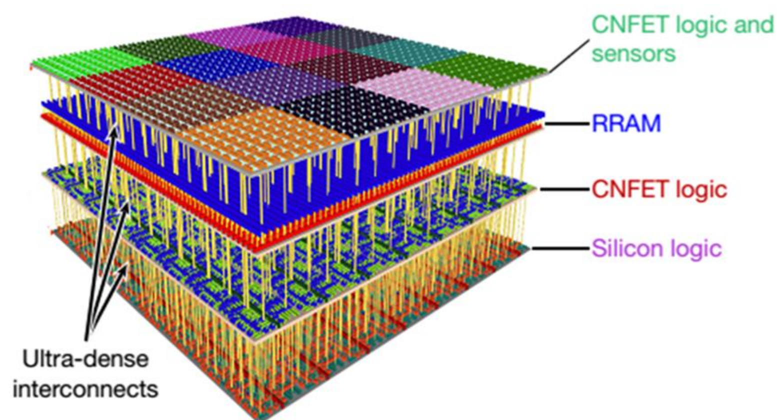


Fig. 2.1 Heterogeneous 3-D integration for hybrid circuits [48]

Heterogeneous integration here not only accommodate circuits with different functionalities in a monolithic manner but also use the hybrid approach to include diverse components like CMOS, CNFETs and RRAM on the same chip. A low-temperature fabrication process (maximum 200ºC) enabled stacking CNFET logic and RRAM on the top of CMOS [48]. In this system more than thousands of

CNFET inverters characterized as gas sensors, provide signals to the computational unit comprised of CNFETs. Another subsystem in a 3-D integrated stack consists of a hybrid memory with select logic using silicon FETs and a row decoding using CNFETs for the RRAM. The primary signal conditioning for the CNFET gas sensor arrays is done by sense amplifiers made from silicon FETs.

Similarly, in their earlier work [49] the researchers demonstrated successful hybrid 3-D integration for an inverter (CNFET pull-up, Si FET pull-down), a two-input NOR gate (CNFET pull-up network, Si FET pull-down network) and cascaded CNFET/CMOS inverter logic. A hybrid circuit for FPGA switchbox with a four-layer approach involving CNFET select transistor, RRAM layers and silicon FET as a routing switch is discussed in [50]. A significant reduction in overall area footprint, as well as energy-delay-product, was achieved with this kind of integration. The remarkable feature of these developments is that the entire fabrication process is in line with and compatible with the CMOS process. Only silicon transistor process including dopant activation is carried out at temperatures exceeding 1000°C while the remaining fabrication steps of RRAM and CNFET fabrication are carried out at relatively lower temperatures without damaging rest of the circuit elements. In order to achieve near perfect alignment, a CNT growth process is first carried out on a quartz substrate and subsequently, the CNTs are transferred on to the chip. This has enabled separation of high-temperature CNT growth process and a relatively low-temperature CNT transfer process. CNTs are grown on quartz substrate nearly at 900°C while the transfer process occurs at just 130°C [50].

With the rapid advances and significant achievements in this field, Gargini, P. A. gave projections for beyond 2020 to sustain Moor’s law by means of Three-

dimensional heterogeneous integration of logic, memory, and other capabilities [51]. IEEE IRDS "International Roadmap for Devices and Systems" Committee (2017) addressed viable emerging devices and novel architectures such as heterogeneous 3D integration by extending the functionality of CMOS [7]. Fig. 2.2 shows a conceptualized hybrid system architecture [52] showing a heterogeneous integration of devices such as 2D FET, 1D CNFET, STT MRAM, 3D RRAM, ultra-dense interconnects, vias and efficient heat removal thermal layers. Almost every aspect of typical VLSI circuits and systems such as computations, memory asses, massive storage, clock and power circuits are to be catered by these complex systems.

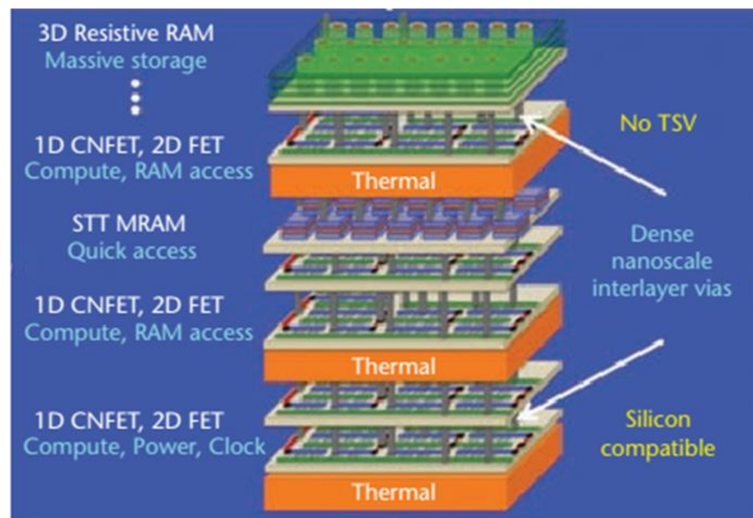


Fig. 2.2 Architecture of 3-D heterogeneous integration with efficient heat removal layers [52]

2.3 CNTs and CNFETs

S. Iijima (1991 and 1993) for the first time reported elucidation of the atomic structure and helical character of multi-wall[17] and single-wall carbon nanotubes[18]. After the discovery of CNTs, enormous interest was created to propose different applications and CNFETs were considered quite promising futuristic devices to be explored as an application of CNTs. The early attempts to fabricate CNFETs [53] were made by using back gate geometry with a single SWNT deposited over the SiO_2 oxide layer and in between two gold electrodes forming the

source-drain contacts. However, this technique lacked basic requirement of VLSI compatible wafer scale manufacturing. To fabricate CNFETs in a large scale, accommodating multiple CNTs on to a device in a VLSI compatible manner, a wafer scaled growth (on quartz substrate) and transfer (on Si substrate) were demonstrated in [54] to achieve more than 99.5% aligned CNT yield.

J. Charlier et al. describes the honeycomb structure of 2-D graphene with lattice vectors. Authors provide an estimation of nanotube diameter from chiral vectors. The paper describes how metallic and semiconducting character of the nanotube is inferred from the honeycomb structure and also discusses the electronic and transport properties of nanotubes[20]. S. Kumar Sinha and S. Chaudhury showed that unlike MOSFETs, in CNFET devices, the effect of temperature on threshold voltage is negligibly small. Results reported shows a negligible V_{th} variation for the temperature range of -25°C to 125°C [55]. Authors in [56] compared CNFET based SRAM cell with CMOS SRAM and showed that CNFET based SRAM cell exhibited 84% less leakage power consumption and less variability to process parameters.

Variability associated with CNFETs is a major obstacle in realizing robust circuit performance. Just like conventional MOSFETs, which show variability in terms of process-voltage-temperature (PVT), CNFETs also suffer from quite unique variability issues posed by flaws in manufacturing CNTs with unique diameters, improper orientation of CNTs, inconsistent doping concentrations in source-drain extension regions, changeable CNT count/density and occurrence of undesired metallic CNTs. H. Shahidipour et al. showed that variations in chirality results in diameter dissimilarities that affect the drive current and the threshold voltage of the CNFETs. Variability in the drive current (I_{ON}) is more significant in CNTs with

lesser mean diameters as compared to larger diameter CNTs. Experimental results point out a Gaussian distribution for the diameter of CNTs grown using different growth techniques [57].

An important milestone achieved in the progress of CNT technology is the development of a primitive CNT computer based on von Neumann architecture[58]. The CNT computer uses appropriately sized 178 number of PCNFETs, can perform simple arithmetic-logic operations, supports multitasking and can handle interrupts. For example, a simple multitasked operation such as the simultaneous execution of the counting process and sorting process can be performed by the computer. Just like any other computer, it uses memory as a peripheral system interfaced using off-chip interconnects. The fabrication process employed ensures robust circuit operation which is immune from imperfections such as misaligned/ inappropriately positioned CNTs, pitch variations, and metallic tubes.

2.4 Spice Compatible Model for CNFETs

J. Deng and H. S. P. Wong developed a compact spice model for CNFETs which serves as a substantially accurate tool for design and verification of CNFET circuits. The model supports CNTs which can be semiconducting or metallic in nature, different chiral vectors and hence different diameter CNTs. The CNFET model exhibits compatibility for analog as well as digital circuits and takes care of various CNT imperfections and non-ideal effects. This model also referred as Stanford model is realized with an HSPICE [38], [59].

CNFET device models have been developed by several research groups. Amongst them, the Stanford model is a compact and accurate HSPICE compatible model calibrated against experimental device data. The model covers important aspects of CNFET including parasitic capacitances, ballistic transport, band structure

physics and inter-channel screening. The model is described in two parts with the first part dealing with the intrinsic channel region of the CNFET considering non-idealities such as optical phonon scattering, charge screening effect in an array of closely spaced CNTs, band to band tunneling while the ac response is characterized by a trans-capacitance network model. The second part as an extension discusses device level model considering additional non-idealities such as channel region elastic scattering, source/drain region resistance/capacitance, Schottky barrier resistance between doped CNT-metal contacts and metal interconnect capacitance. Analysis, comparison and benchmarking with standard CMOS library cells was also done to validate model accuracy against the experimental data.

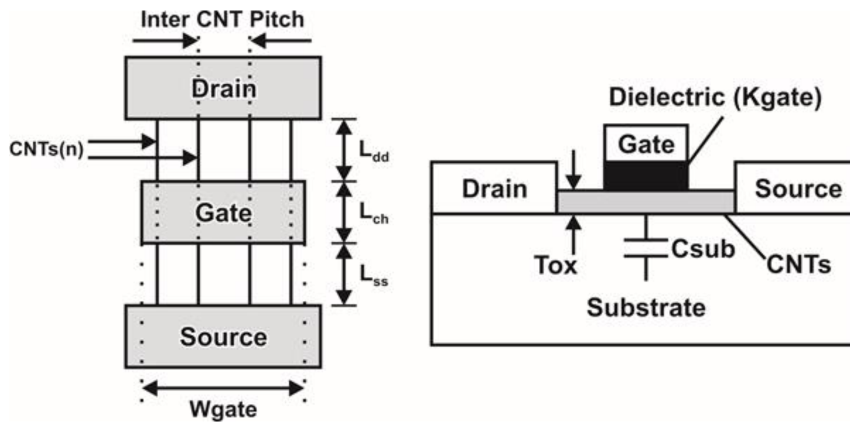


Fig. 2.3 CNFET model with parameters

As per the model CNFET device can be instantiated in the HSPICE deck with a syntax similar for instantiating CMOS device. Figure 2.3 shows the HSPICE compatible device model with relevant parameters. Typical device instantiation with parameter values in the HSPICE deck for NCNFET can be,

XCNT1 Drain Gate Source Substrate NCNFET L_{ch}=32e-9 L_{ss}=32e-9 L_{dd}=32e-9 K_{gate}=16 T_{ox}=4e-9 C_{sub}=40e-12 Pitch=20e-9 n1=19 n2=0 tubes=3.

Where L_{ch} is the channel length which corresponds to exact length of individual intrinsic single-wall carbon nanotubes placed beneath the gate of CNFET, L_{ss} is the

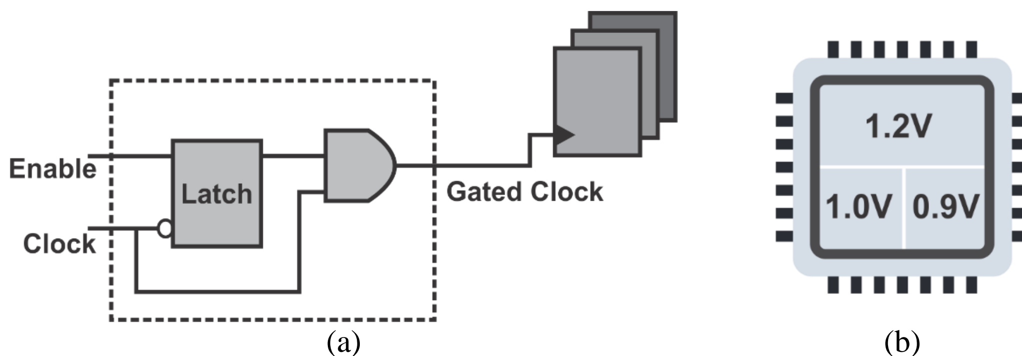
length of CNTs outside the top gate extended towards the source (source side extension region), L_{dd} is the length of CNTs outside the top gate extended towards the drain (drain side extension region), K_{gate} and T_{ox} being the dielectric constant and oxide thickness respectively, C_{sub} is the coupling capacitance, the distance between adjacent tubes beneath the gates is referred to as inter CNT Pitch, n1, n2 are chiral vectors and tubes equals to number of CNTs used. The important model parameters are listed in Appendix C.

2.5 Low Power Techniques

Low-power design drew attention beginning in 1990 and the quest to design with ultra-low power techniques continues to dominate the research in different application domains. During those years researchers have brought several distinctive power-saving approaches while managing the tradeoff between performance and power consumption. Both static and dynamic power dissipation has to be systematically addressed to satisfy the power requirement of energy constrained systems. Various device, circuit, and architectural level measures to minimize dynamic power consumption such as transistor sizing, gate sizing, dual power supply, clock gating, multi-voltage operation, parallelism and pipelining can be employed to address the problem. With these techniques power consumption of high-performance digital systems such as microprocessors, digital signal processors can be minimized.

The dual power supply is a technique that significantly reduces dynamic power dissipation by choosing a lower power supply for sub-circuits having non-critical delay paths without compromising on performance [60]. Selective gate sizing to increase gate delays for non-critical paths in a circuit is an effective measure to tackle dynamic power dissipation in digital circuits [61]. Just like gate sizing

wherein devices within a gate are sized uniformly, one can opt for transistor sizing with independently sized devices to optimize speed-power trade-off [62]. In a clock gating approach (Fig. 2.4(a)) to minimize dynamic power dissipation, the clock signal is disabled for a period when data in a circuit block is not changing. Similar to dual supply technique one can use more than two power supply levels (eg. 0.9V, 1V, 1.5V) depending upon performance requirements of individual subcircuit blocks resulting in significant dynamic power dissipation. This approach of dynamic power reduction is called multi-voltage technique (Fig. 2.4(b)).



(a) (b)

Fig. 2.4 (a) Clock gating and (b) Multi-voltage technique

Pipelining is an effective method which allows simultaneous voltage scaling. In a pipelined circuit architecture with M stages critical path is reduced to 1/M of its original length and capacitance is reduced by a factor C/M in a single clock cycle. Parallel processing architecture replicates the hardware to obtain the same throughput while reducing both supply voltage and clock speeds ie- effectively slowing down identical circuit blocks which collectively (multiplexed) provide necessary throughput [63].

In an era of aggressively scaled devices, in a nanometer regime, subthreshold leakage and gate leakage are contributing significantly in the overall power consumption of handled/portable, wearable, implantable electronic devices and gadgets. Various leakage components [64] in a nano-scaled NMOS transistor such

as gate leakage, hot carrier injection, gate induced drain leakage (GIDL), punch through effect, subthreshold leakage, band to band tunneling, reverse biased p-n junction current are shown in Fig. 2.5.

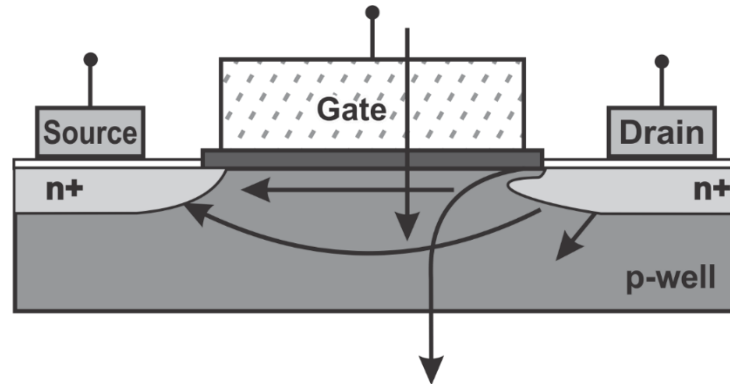


Fig. 2.5 Leakage mechanisms in aggressively scaled transistors [64]

Minimization of leakage currents has now become a priority design aspect for the portable electronic systems which are either battery powered or scavenge energy from the surroundings. Techniques described in this section cater to the need of most of the battery powered systems so as to provide high performance while active and low leakage while idle. The techniques used to tackle leakage power consumption includes a power gating scheme, variable V_{th} by means of substrate biasing, adaptive body biasing technique, stacked transistors etc. These techniques find great applications in case of the energy scavenging systems wherein ultra-low power consumption is of more significance rather than achieving high performance.

The power gating scheme [65] uses meticulously sized sleep transistors (high V_{th}) placed in series with the logic block transistors (low V_{th}). The scheme is depicted in Fig. 2.6(a). The high V_{th} sleep control switches would obviously leak substantially less current in their off state when the circuit block is put in standby/power saving/sleep mode. The scheme can be realized in different manners such as coarse grain, fine grain or clustered approach. In spite of being an effective measure to reduce leakage power, power gating involves an extra effort in properly

sizing sleep transistor switches, introduces gate-level delay degradation, overall delay degradation and obviously, an increased area is required to accommodate sleep transistors. However, a novel hybrid power gating scheme as shown in Fig. 2.6(b), reported in [44] overcomes these limitations to some extent by introducing a new device such as CNFET power gating switches as a replacement to CMOS power gating switches.

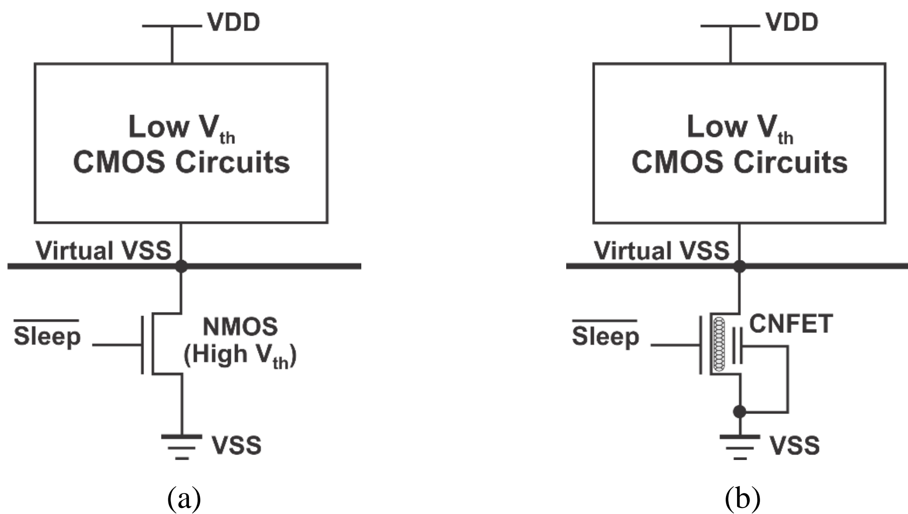


Fig. 2.6 (a) Conventional power Gating (b) Hybrid power gating

Twin or triple-well process and body effect allow us to employ a variable V_{th} (VTCMOS) scheme wherein substrate bias control is used to configure high V_{th} in a standby mode while low V_{th} in a normal high-performance mode [66]. The VTCMOS scheme is shown in Fig. 2.7(a). Another technique that exploits body effect for subthreshold leakage reduction is the adaptive body bias of transistors [67]. Based on switching speed or clock frequency requirement of a typical functional block, the adaptive body bias generator decides appropriate biasing which results in low V_{th} devices being used for high switching frequency functional blocks and high V_{th} devices for low switching frequency functional blocks. A stack of transistors in series (Fig. 2.7(a)) results in less leakage current. Various stacking

strategies such as simple transistor stack [68], forced transistor stacking [69] and sleepy stack [70] are also employed to deal with excessive subthreshold leakage.

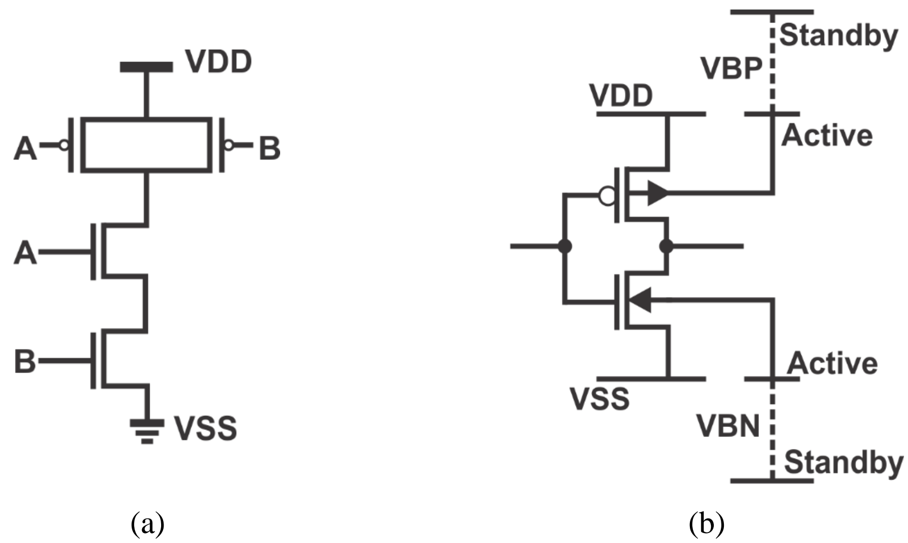


Fig. 2.7 (a) Stacking effect in a logic gate and (b) VTCMOS technique

In a forced transistor stacking as shown in Fig. 2.8(a), instead of using a single large transistor (width W) two half sized transistors (width W/2) in series are used which results in less leakage but at the cost of slowing down the circuit. Sleepy track approach that is shown in Fig. 2.8(b), inserts a sleep transistor with sleep control pins in parallel with two forced stacked transistors. The sleep transistor operates in active mode and switched off during sleep mode.

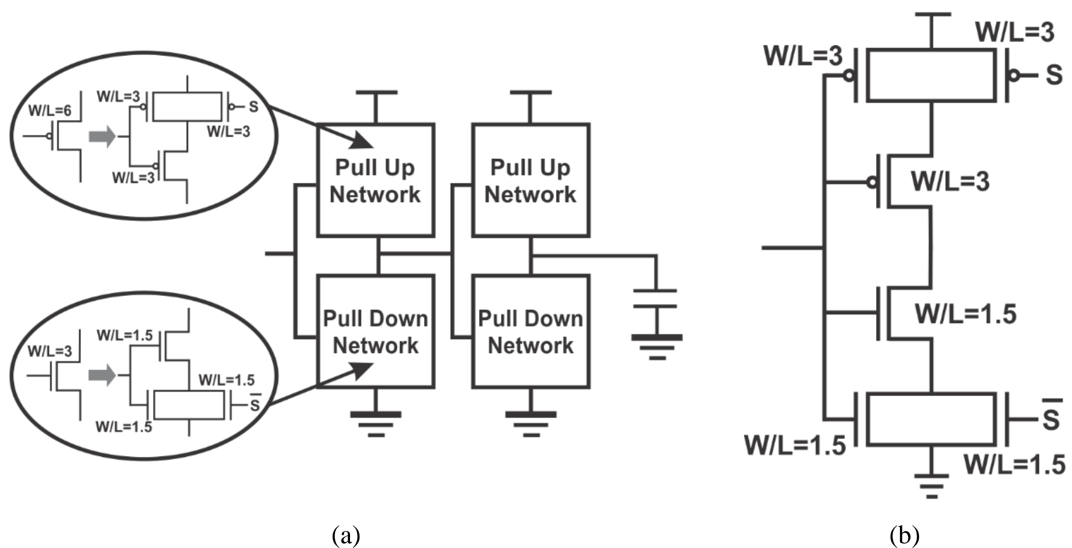


Fig. 2.8 (a) Forced transistor stacking and (b) Sleepy stack using parallel sleep transistors

The techniques described in this literature review cater to analog as well as digital circuit domains and particularly ultra-low-power systems. M. Alioto, presented energy and power requirements for ultra-low-power systems. Important findings summarized by the author were- the nominal V_{dd-min} should be substantially higher than theoretical limits to account for variability, aggressive pipelining is a useful technique to further decrease the energy per operation but parallelism is less effective in the subthreshold regime [1]. R. Sarpeshkar presents fundamental principles and techniques for ultra-low power circuit design and their applications in biomedical electronics. Subthreshold operation is the most promising approach for ULP biomedical circuits [71]. C. Galup-Montoro et al. presented ultra-low voltage operation of CMOS analog circuits: oscillators, rectifiers and amplifiers. Authors showed that analog circuits, such as oscillators built around zero-V_{th} MOSFET, can operate with supply voltages below thermal voltage kT/q [3]. S. R. Shridhara describes ultra-low-power microcontroller for portable wearable and implantable medical electronics. The implemented epileptic seizure onset detection system consumed less than 1 μW at a supply voltage of 0.8V [2]. It is expected that device and interconnect scaling should go hand in hand and ultra-low-power design efforts should include interconnect design issues as well. S. Pable et al. addressed interconnect design issues in the subthreshold regime and compared SWCNT, Copper, and mixed SWCNT-MWCNT bundle interconnects. Authors showed that local (short length) SWCNT interconnects outperform copper interconnects in the subthreshold regime [72].

2.6 Summary

The literature review in the context of this research is provided in this chapter. It is revealed from this review that the challenges in reducing power consumption can be

overcome by employing techniques involving multiple domains such as effective use of emerging devices in pure or hybrid circuit topologies, low voltage techniques, subthreshold operation, both dynamic and leakage power reduction techniques. This also implies a great necessity to do further research that exploits novel properties of emerging nanoelectronics devices to solve existing problems.

Chapter 3

HYBRID CMOS-CNFET VOLTAGE CONTROLLED OSCILLATOR

3.1 Introduction

This chapter presents a hybrid CMOS-CNFET voltage controlled oscillator (VCO) with low power dissipation and linear response over a wide control voltage range. The hybrid circuit is based on Predictive Technology Model (PTM) 32nm low power CMOS devices and 32nm CNFET devices with different threshold voltages. The VCO frequency and power dissipation are investigated for CNFET parameters such as the number of nano-tubes, gate oxide thickness, inter CNT pitch and chiral vectors. The linearization of VCO response is achieved using a hybrid CMOS-CNFET device combination without needing a resistor or a wide device. The circuit exhibits excellent linearity as compared to pure CMOS circuit over a tuning range from 84MHz to 1.6GHz corresponding to a control voltage range from 0.3V to 0.8V. The VCO power dissipation is confined within sub 15µW range for control voltages up to 0.6V. Following sections in this chapter cover a review of Voltage Controlled Oscillators, description of the hybrid-CMOS CNFET VCO with relevant analysis and performance comparison with pure CMOS implementation. Effect of CNFET parameters on VCO frequency and power dissipation is also presented in the subsequent section.

3.2 Voltage Controlled Oscillators (VCOs)

VCOs produce an AC output signal whose frequency can be varied in a controlled manner using a DC voltage signal. They are the widely used building

blocks in analog and mixed-signal electronic circuits such as Phase-Locked Loops (PLLs), analog to digital converters (ADCs), radio frequency integrated circuits (RFICs), RFIDs and many other mixed circuits [73], [74]. Most of the VCO topologies cater to high-frequency applications, however, there exists a special class of applications such as biomedical, audio frequency and robotic control wherein the frequency range of less than a Hertz to few kilohertz is required. VCO designs mainly comprise topologies such as LC tank oscillators and ring oscillator VCOs. Ring oscillator VCOs provide comparatively wider tuning range in PLL applications, occupy lesser silicon area as compared to LC tank oscillators and are better suited for silicon integration[75]. However, LC tank oscillator based PLL designs exhibit better phase noise performance as compared to ring oscillator VCOs [76], [77]. Unlike LC tank oscillators, ring oscillator VCOs do not need passives like high-quality inductors and hence can be easily integrated on to chips using standard CMOS process. A commonly used ring oscillator based VCO topology is a current starved voltage controlled oscillator (CSVCO) which consists of several numbers of VCO stages comprising of current starvation stages and inverters [78]. As compared to CSVCO, Schmitt trigger based VCO needs a single VCO stage, a Schmitt trigger with hysteresis and a single inverter resulting in less number of transistors required for the circuit.

A VCO with wide linear response are excellent candidates to realize ADCs that convert VCO frequency into binary digital information [79]. This conversion is achieved by counting rising or falling edges of VCO output waveform and further feeding the count to a simple register. Counting is performed by allowing pulses of VCO output waveform to pass through an AND gate for a specific interval of time resulting in frequency to digital conversion. In VCO based ADCs the linearity error

which is expressed as the largest deviation from the best fitting straight line over the VCO response imposes a limit on quantization steps and hence limits the resolution of the ADC [79]. More is the linearity error less is the number of quantization levels and less is the resolution. This implies that a VCO linearity plays an important role in deciding the accuracy of VCO based ADCs and hence it becomes essential to design a VCO that gives linear response over wide control voltage range. The wide and linear tuning range is also a predominant requirement of VCOs (and hence PLLs) incorporated into RFIDs. Typical VCO responses depicting useful input voltage range and linearity error are shown in Fig. 3.1. VCO being the key component and the most power consuming block of PLL, curtailing the power consumption in VCOs results in significant overall power reduction in PLLs employed in RFICs.

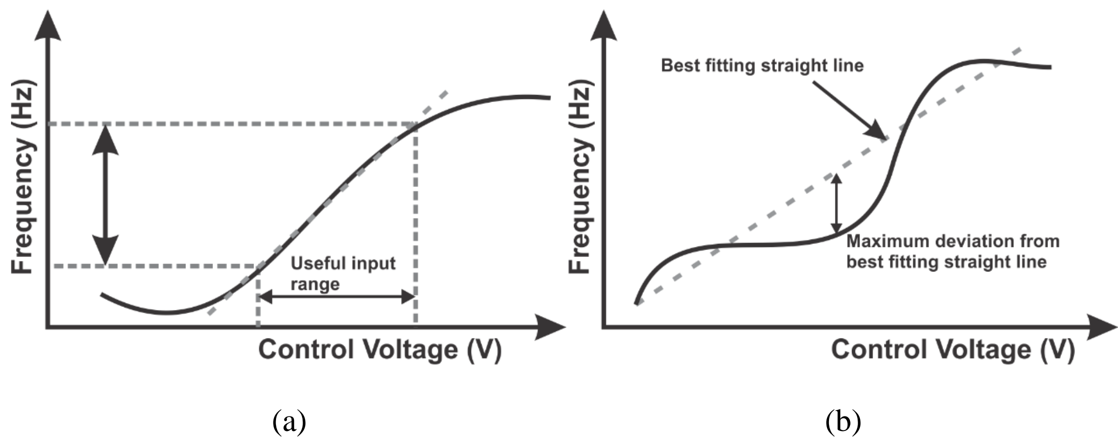


Fig. 3.1 (a) Tuning range, output frequency range and (b) linearity error in VCO

3.3 Hybrid CMOS-CNFET VCO

In this section, we present Schmitt trigger based voltage controlled oscillator that uses hybrid CMOS and CNFET approach. The proposed hybrid circuit is optimized to achieve better linearity and reduced power dissipation as compared to pure CMOS circuit. Simulations of the proposed VCO are performed in an HSPICE environment. Future of the nano-electronic systems relies on the novel monolithic

3D integration of heterogeneous circuits such as computational elements, memory, RF and analog building blocks. Such type of 3D integrated systems having futuristic applications have been reported in [80], wherein researchers reported vertically stacked integrated circuit layers involving hybrid co-integration of CNFET logic blocks and conventional silicon CMOS logic blocks. Proposed hybrid CMOS-CNFET VCO circuit consisting of both CMOS and CNFET devices is a potential candidate for futuristic 3D integrated monolithic chips.

Ring oscillator VCOs consists of n-number of stages with each stage contributing to the overall nonlinearity of the VCO. To overcome this issue the topology given in Fig. 3.2 can be employed wherein a single current starvation stage followed by a Schmitt trigger with hysteresis is used. One of the applications of Schmitt trigger is an RC oscillator. Similarly, a Schmitt trigger along with current sources can form a voltage controlled oscillator. The proposed design utilizes CNFETs for the construction of the Schmitt trigger. The upper two stacked p-type CNFETS (M10, M9) and lower two n-type CNFETs (M8, M7) form an inverter while CNFETs M12, M11 work as feedback transistors. The Schmitt trigger output is at V_{DD} until a switching occurs. Switching occurs when the voltage across the charging capacitor (input of Schmitt trigger) rises by a threshold voltage of M8 than the voltage at the junction formed between the lower stack of CNFETs. The higher and lower switching point voltage levels of Schmitt trigger hysteresis are decided by the threshold voltages of stacked CNFETs. Also transistors M1 and M4 are CNFETs which act as current sources mirroring the currents in MOSFETs M5 and M6. The inverter is realized using conventional MOSFETs. The 32nm channel length CNFETs with a chiral vector of (17,0) corresponding to a threshold voltage of 0.323V have been chosen. The number of tubes equal to 3 with inter CNT pitch of

4nm is used. PTM LP 32nm model is chosen for the MOSFETs. MOSFETs used in the hybrid implementation are sized with W/L=10.

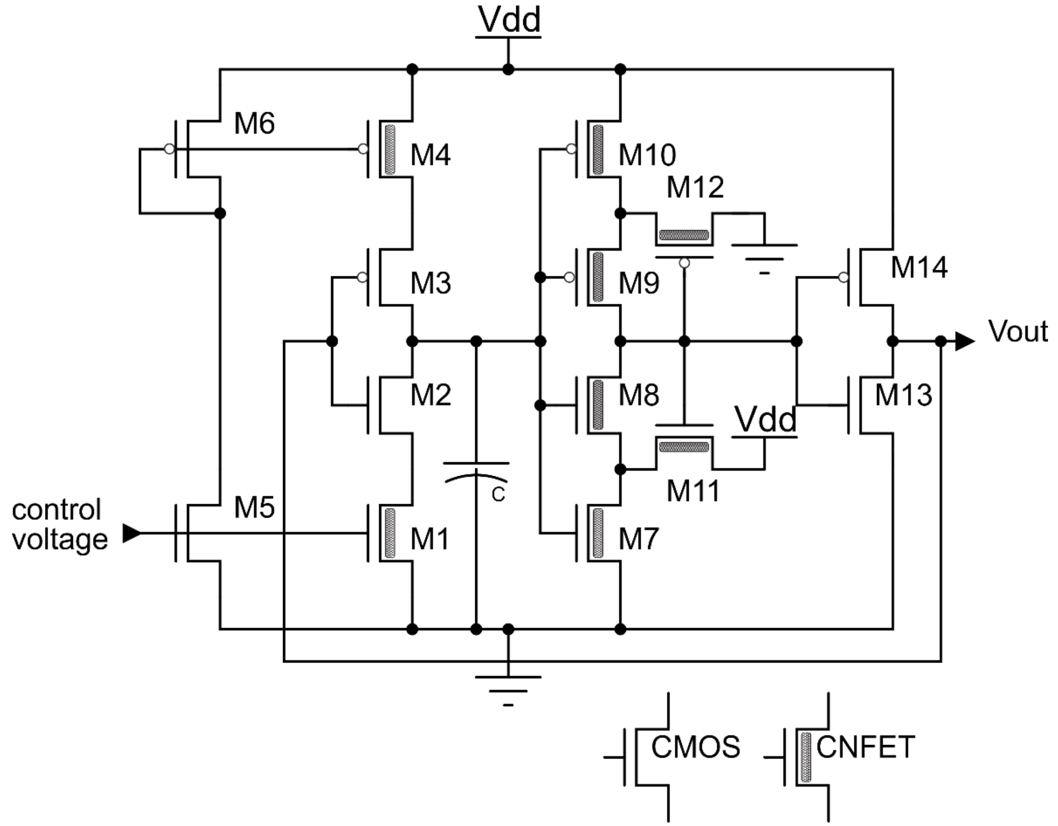


Fig. 3.2 Hybrid CMOS and CNFET VCO

The Schmitt trigger circuit uses equally sized CNFETs with a gate width of 40nm and channel lengths of 32nm. If V_{SPH} and V_{SPL} are higher switching point and lower switching point voltages respectively and V_{THN} and V_{THP} are threshold voltages of NCNFET and PCNFET respectively then we can write,

$$\left[\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2 = \frac{W_7 L_{11}}{L_7 W_{11}} \tag{3.1}$$

$$\left[\frac{V_{SPL}}{V_{DD} - V_{SPL} - V_{THP}}\right]^2 = \frac{W_{10} L_{12}}{L_{10} W_{12}} \tag{3.2}$$

For equally sized CNFETs,

$$\left[\frac{V_{DD} - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2 = 1 \tag{3.3}$$

$$\left[\frac{V_{SPL}}{V_{DD} - V_{SPL} - V_{THP}}\right]^2 = 1 \tag{3.4}$$

Rewriting equations 3.3 and 3.4 we obtain V_{SPH} *and* V_{SPL} respectively. Further (17, 0) chiral vector used for CNTs corresponds to a V_{th} of 0.323V for the CNFETs. Substituting, $V_{THN} = V_{THP} = 0.323V$ we get the higher and lower switching point voltages V_{SPH} *and* V_{SPL} respectively for the CNFET based Schmitt trigger.

$$V_{SPH} = \frac{V_{DD} + V_{THN}}{2} = \frac{1 + 0.323}{2} = 0.6615V \tag{3.5}$$

$$V_{SPL} = \frac{V_{DD} - V_{THP}}{2} = \frac{1 - 0.323}{2} = 0.3385V \tag{3.6}$$

The oscillations produced by the circuit for VCO control voltage of 0.3V are shown in Fig. 3.3. The frequency f_{osc} can be found with an expression.

$$f_{osc} = \frac{1}{C\, V_{hyst}\left(\frac{1}{I_{DM1}} - \frac{1}{I_{DM4}}\right)} \tag{3.7}$$

The Schmitt trigger hysteresis $(V_{SPH} - V_{SPL})$ of 0.323V results in the capacitor to charge and discharge between V_{SPL} and V_{SPH} producing sustained oscillations.

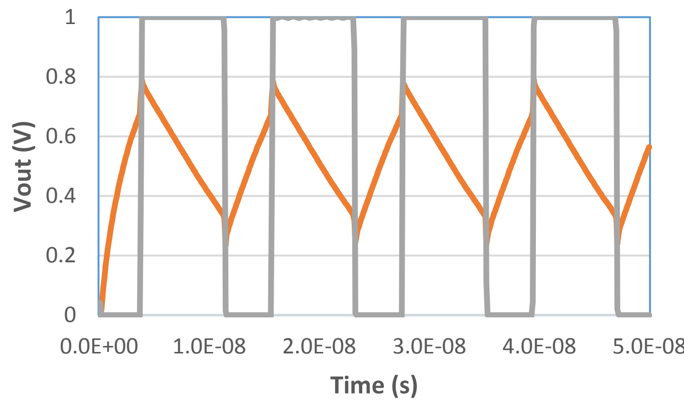


Fig. 3.3 Output waveform of hybrid CMOS-CNFET VCO

3.4 Results and Discussion

One of the prime requirement of a VCO for PLL applications is wide and linear tuning range. Fig. 3.4 shows the VCO oscillation frequency as a function of the

control voltage for CMOS implementations and a hybrid CMOS-CNFET implementation. The hybrid circuit exhibits a better linear response as compared to pure CMOS circuit (Fig. 3.4).

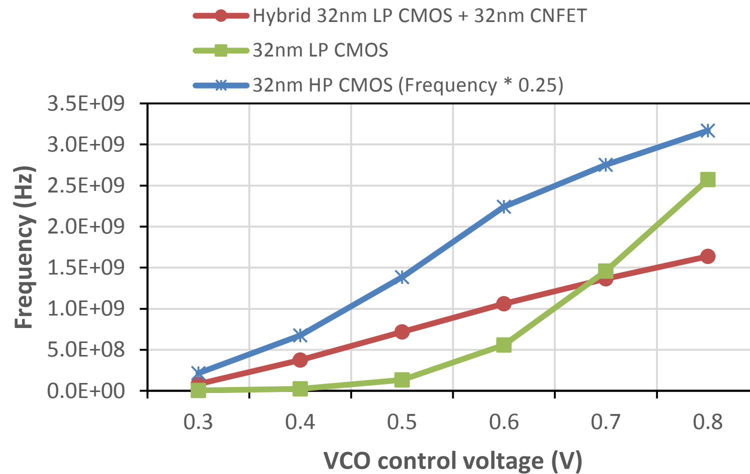


Fig. 3.4 Frequency vs VCO control voltage for hybrid and CMOS VCOs

The nonlinear response in pure CMOS circuit is because of high V_{th} devices being used for reduction in power dissipation. Use of high-performance low V_{th} devices yields in better linearity at the cost of higher power dissipation. The hybrid circuit compensates the nonlinearity produced by the transistor M5 which is under weak inversion (sub-threshold conduction) for control voltage below V_{THN}. The compensation is achieved by replacing CMOS transistors M1 and M4 by CNFETs and realizing a CNFET Schmitt trigger. Often a linearization technique based on a resistor and a wide CMOS device is used in the VCO designs. However, the proposed hybrid circuit does not need a resistor or a wide device for achieving a linear response.

Comparison of VCOs realized using different technology nodes with hybrid CMOS-CNFET VCO is shown in Table 3.1 (VCO control voltage varied from 0.3V to 0.8V). The hybrid VCO provides relatively smaller gain (K_{vco}) which is desired in low jitter PLL applications. Referring to Table 3.1, Fig. 3.4 and Fig. 3.5 it can be

seen that the hybrid circuit dissipates less power and generates a higher frequency for the same control voltage.

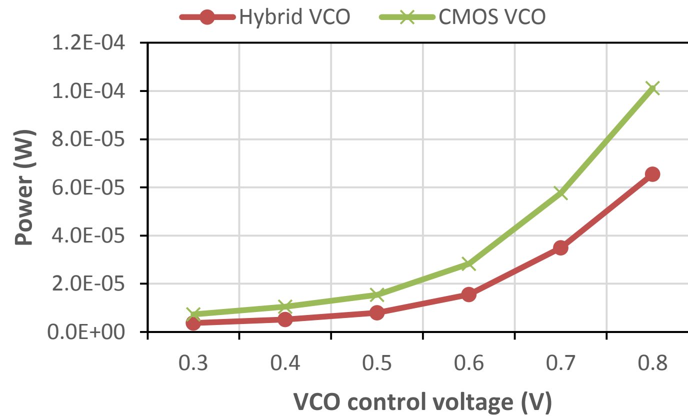


Fig. 3.5 Power dissipation vs VCO control voltage for hybrid and CMOS VCO

Table 3.1: A comparison of proposed VCO with conventional CMOS VCOs

VCO	f_{min}	f_{max}	K_{vco}	Min. Power Diss.		Max. Power Diss.	
CMOS 32nm LP	3.1MHz	2.5GHz	5.14MHz/mV	7.2μW	2.3μW/MHz	101.1μW	0.04μW/MHz
CMOS 32nm HP	858.4MHz	12.6GHz	148MHz/mV	126μW	0.14μW/MHz	480μW	0.03μW/MHz
CMOS 50nm	389.9MHz	2.7GHz	4.61MHz/mV	94.1μW	0.24μW/MHz	298.9μW	0.11μW/MHz
Hybrid	84.0MHz	1.6GHz	3.10MHz/mV	3.6μW	0.04μW/MHz	65.4μW	0.04μW/MHz
Pure CNFET	157.3MHz	6.08GHz	74.4MHz/mV	3.9μW	0.02μW/MHz	23.2μW	0.003μW/MHz

3.5 Effect of CNFET Parameter Variation on VCO Frequency and Power Dissipation

The proposed circuit is investigated for the generated frequency and power dissipation under variations in parameters such as control voltage, number of tubes in the CNFETs, gate oxide thickness, CNFET chiral vectors (threshold voltage) and inter CNT pitch. The oscillator frequency varies linearly with increasing the number of nanotubes in a CNFET for a given control voltage (Fig. 3.6). This gives a simple way to scale the VCO frequency at design time to satisfy VCO specifications for a

PLL application. The thin gate oxide in a CNFET results in a higher transconductance and drive current [81], [82]. Fig. 3.7 shows the effect of gate oxide thickness on the frequency and power dissipation in a hybrid VCO. For low power VCOs relatively higher gate oxide thickness can be used to reduce drive current and achieve reduced dynamic power consumption.

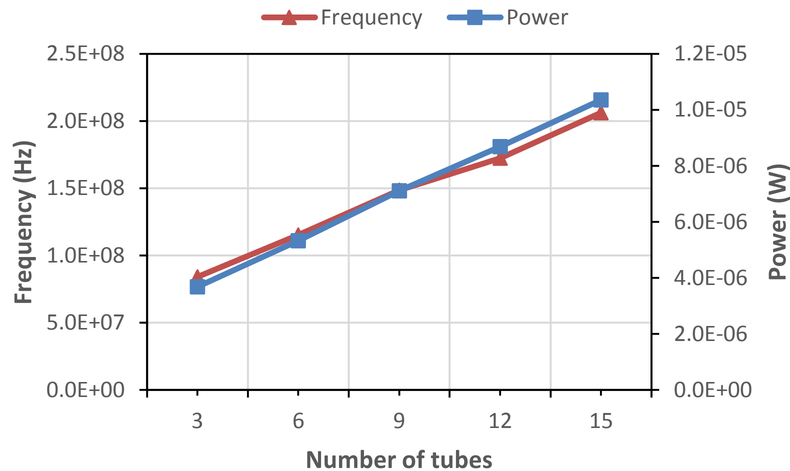


Fig. 3.6 Effect of number of tubes in CNFET on the frequency and power dissipation for a hybrid VCO

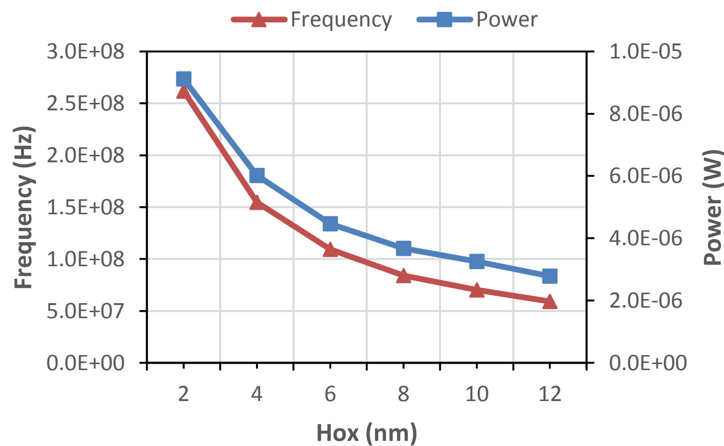


Fig.3.7 Effect of CNFET gate oxide thickness on VCO frequency and power dissipation for a hybrid VCO.

For a fixed width CNFET increasing the nanotube density ie. Decreasing inter CNT pitch results in screening amongst parallel CNTs affecting gate to channel

capacitance and current drive. The drive current remains constant for both middle and edge CNTs if inter CNT pitch is greater than 20nm. Decreasing the inter CNT pitch below 20nm results in reduced dive current with middle CNT current decreasing at a faster rate than that of the edge CNTs [41], [59]. Hence in our circuit decreasing the pitch causes the drive current to decrease, resulting in decreased oscillation frequency and reduced power dissipation (Fig. 3.8).

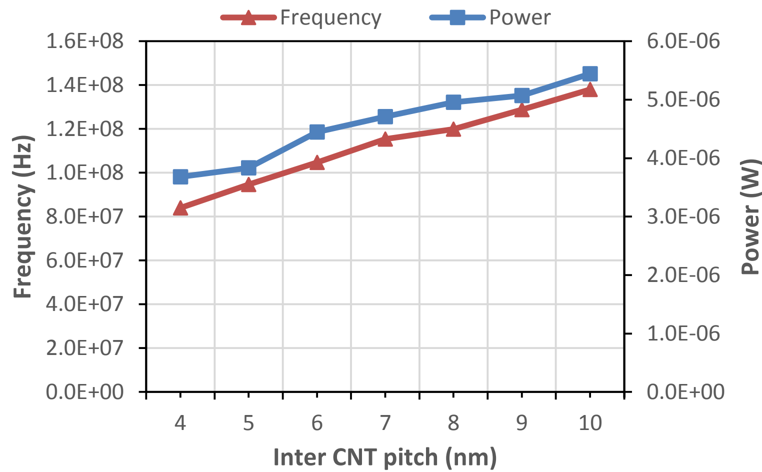


Fig. 3.8 Effect of inter CNT pitch on VCO frequency and power dissipation for a hybrid VCO

The hybrid circuit is also investigated for different CNFET threshold voltages. CNFET threshold voltage is inversely related to the diameter of the CNT. The diameter depends upon the chiral vector denoted by two indices (n, m). The diameter and the threshold voltage (V_{th}) of the CNFET can be calculated using equations 3.8 and 3.9.

$$D_{CNT} = \frac{a_0\sqrt{3}}{\pi}\sqrt{n^2 + nm + m^2} \tag{3.8}$$

$$V_{th} = \frac{\sqrt{3}}{3}\frac{a\,V_{\pi}}{eD_{CNT}} \tag{3.9}$$

Where a0 (0.142nm) is the inter-atomic distance between each carbon atom and its neighbor, a (2.49Å) is the lattice constant, Vπ (3.033eV) is the carbon π-π bond energy, e is the unit electron charge. Fig. 3.9 shows the frequency and power dissipation for the hybrid VCO at different CNFET threshold voltages for a VCO

control voltage of 0.3V. The hybrid circuit is investigated for a set of chiral vectors/threshold voltages (26, 0) / 0.220V, (23, 0) /0 .250V, (20, 0) / 0.289V, (17, 0) / 0323V and (14, 0), 0.392V. Higher the CNFET V_{th}, oscillation frequency and power dissipated by the hybrid VCO decreases accordingly.

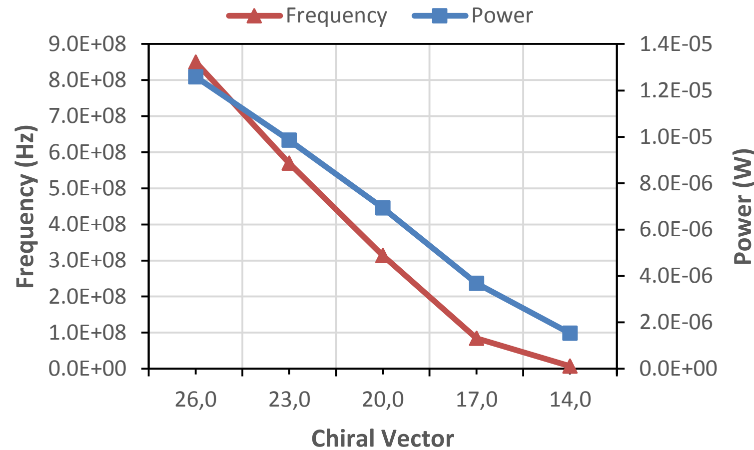


Fig. 3.9 Effect of the chiral vector (threshold voltage) on the frequency and power dissipation for hybrid VCO

3.6 Summary

Hybrid CMOS-CNFET VCO using Schmitt trigger and current sources is presented in this chapter. The VCO was optimized for minimum dynamic power consumption by suitably adjusting CNFET parameters such as threshold voltage (chirality), inter CNT pitch, gate oxide thickness and number of nanotubes. The hybrid topology with 32nm LP CMOS devices and 32nm CNFETs having chirality of (17,0), inter CNT pitch of 4nm, gate oxide thickness of 8nm were found to be optimum for minimizing power dissipation. The VCO oscillation frequency can be tuned linearly with a gain of 3.1MHz/mV from 84MHz to 1.6GHz. The minimum and maximum power dissipation were 3.6µW to 65.4µW respectively. This type of hybrid co-integration of CMOS and CNFET devices can form a basis for the futuristic 3D integrated monolithic chips.

Chapter 4

HYBRID CMOS-CNFET OTA-C FILTERS

4.1 Introduction

Analog filters for biomedical signal processing applications deal with very slow or low-frequency electrical activities of the physiological signals. This chapter describes first order, second order, fifth order elliptic low pass, second-order notch and high pass OTA-C filters using hybrid CMOS-CNFET technology. CNFETs and CMOS devises can be heterogeneously integrated on a single 3-D chip to realize important signal processing building blocks such as OTA-C filters. Proposed circuits use hybrid CMOS-CNFET Operational Transconductance Amplifier (OTA) as a building block for OTA-C filters. Realized filter circuits satisfy ultra-low power consumption requirement of wearable and implantable biomedical devices. The transistors used in the circuit operate in weak inversion to achieve ultra-low power consumption. In this chapter, we put forward OTA-C filter designs based on hybrid CMOS-CNFET OTA. Subsequent sections in this chapter describe a brief review of biomedical filters (Section 4.2), followed by hybrid CMOS-CNFET OTA (Section 4.3), OTA-C filter realizations (Section 4.4) and simulation results with discussion (Section 4.5).

4.2 Biomedical Filters

Filters enhance the signal quality by preserving the signal of interest and at the same time systematically reject unwanted noise and interference. Real world signals including biomedical signals are almost always susceptible to unwanted noise, interference, and artifacts unless filtered properly. Different types of filters can be employed to deal with these noise, interference, and artifacts. In case of biomedical

signals, often the frequency spectra of the signal of interest overlap with that of noise components and signal artifacts. This makes biomedical filtering a difficult task. Furthermore, biomedical electronic devices (including biomedical filters) needs to abide by different regulations imposed by the International Electrotechnical Commission (IEC), Federal Communications Commissions (FCC), regarding safety and quality control requirements. Different types of filters based on their ability to reject certain frequency bands and to faithfully pass certain frequency bands with a transition region in between are shown in Fig. 4.1.

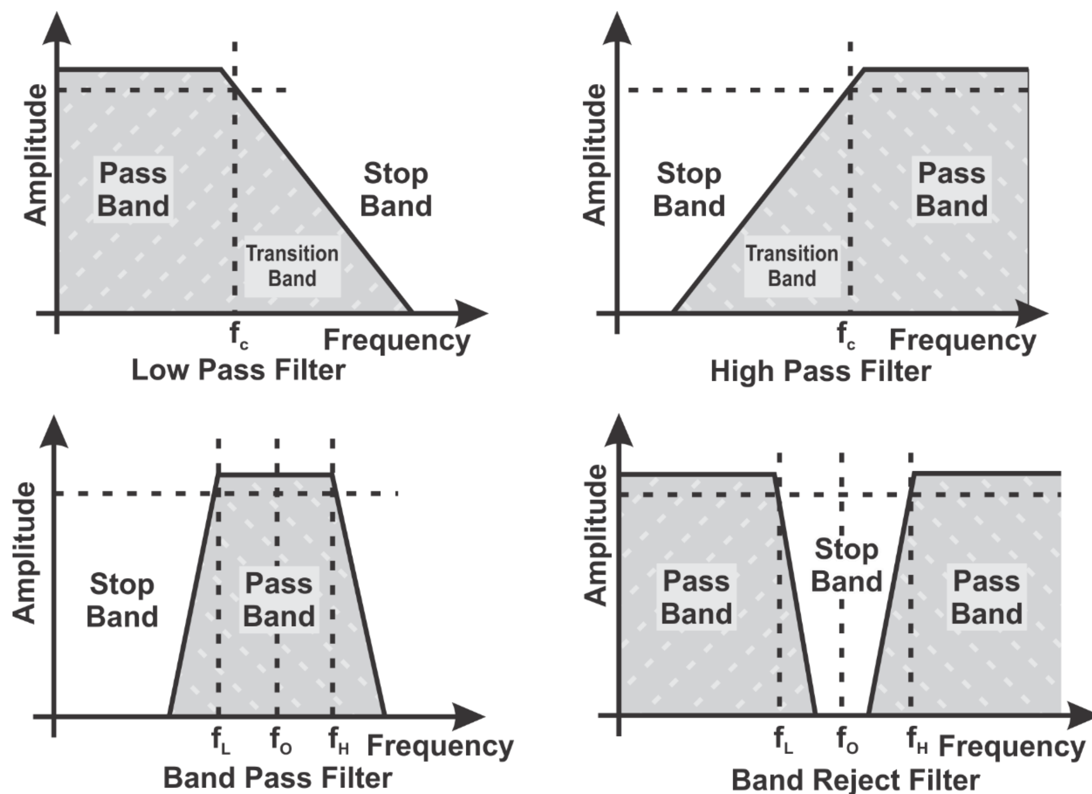


Fig.4.1 Different types of filters with a transition region between the passband and stop bands

Different applications demand different kind of filtering requirements such as low pass (ideally no change for frequency components below cut-off and maximally attenuating frequency components above cut-off), high pass (ideally no change for frequency components above cut-off and maximally attenuating frequency components below cut-off), bandpass (ideally no change for frequency components

within a selective narrow or wideband and maximally attenuating rest of the frequency components), band reject (ideally maximally attenuating a selective narrow band of frequency components and no change for rest of the frequency components). The transition region (band) is always present in practically realized filters because of inherent non-ideal nature of both analog and digital filters. Ideally one should strive to design a filter without a transition band and the one which is having very sharp or abrupt transitions between pass bands and stop bands. However, narrower the transition width, more is the presence of ripples in the pass bands and stop bands. There exists a tradeoff amid maximally flat passbands and transition widths.

Filters can be analog or digital filters. Analog filters deal with continuously varying signals while digital filters process sampled data. Analog filters include passive filters utilizing passives such as inductors, capacitors and resistors. Analog active filters are built around operational amplifiers (OPAMPS) or operational transconductance amplifiers (OTA). Active filters include active RC filters, OTA-C filters, LC filters and switched capacitor filters. OPAMP based active RC filters offer better dynamic range and linear characteristics at the price of increased power dissipation and area overhead. Switched capacitor filters exhibit excessive leakage issues in the ultra-scaled regime. Amongst the different type of active filters, OTA-C filters provide wide frequency range for the desired filter cut off frequencies. OTAs form the basic building block of OTA-C filters. OTA-C filters are better suited for on-chip integration with a simple way to do frequency tuning either by changing OTA transconductance or by choosing suitable capacitor values [83]. The OTA -C filters find applications in many biomedical signal processing applications. Examples include Electrocardiogram (ECG) [84], bionic ear [85], neural recording

interfaces [86], and electroencephalogram (EEG) [87]. The OTA-C filters are the better choice for analog front ends of biomedical systems involving low-frequency physiological signals.

4.3 Hybrid CMOS-CNFET Transconductor

A transconductor (OTA) which is realized with a hybrid CMOS-CNFET approach is discussed in this section. CNFET is one of the promising alternatives to the conventional CMOS technology in the sub 10nm regime while at the same time provide an opportunity for hybrid co-integration in a complementary manner. Owing to its superior material and electrical properties along with CMOS fabrication compatibility, CNFET/hybrid CMOS-CNFET circuits show enormous potential for the emerging nano-electronic circuits. Such type of hybrid architectures is a promising approach for wearable and implantable biomedical devices. To utilize these technological advances up to full potential one needs to explore the applicability of this technology for analog domain involving analog front-end amplifiers, filters and signal processing. Based on this approach, we have proposed a transconductor (OTA) which is realized as a hybrid circuit with P-type CMOS transistors and N-type CNFETs for the OTA-C filters. Fig. 4.2 shows the realized transconductor. The circuit comprises a differential amplifier as its core accepting two inputs (V_p and V_m), biasing (V_b) and current mirror circuits as its load. The HSPICE circuit simulation tool is used to simulate the realized OTA-C filters. CMOS transistors are modeled as per Predictive Technology Model (PTM) 32nm low power device technology while the CNFET devices use Stanford University compact spice model [38], [59]. The transistors are sized as W=100, L=2 (PMOS) and (19, 0) chiral vector with 3 number of CNTs for N-CNFETs. CNFETs offer several benefits over CMOS with regards to higher drive current, lesser process

variations and less leakage current. The output current expression of the transconductor is given by,

$$I_{out} = g_m(V_p - V_m) \quad (4.1)$$

Where g_m is the transconductance of the OTA. The OTAs can only drive capacitive loads and do not require to bias the resistive elements and output driver circuits resulting in a circuit with both its inputs and outputs as very high impedance node. This makes the OTA act as a voltage controlled current source. The OTAs of this kind are the circuits of choice for biomedical signal processing applications such as neural amplifiers for electrocorticograms and electroneurograms [88]. Weak inversion or subthreshold operation of the transistors minimizes their transconductances and also improves the transconductor linearity. To minimize the OTA transconductance and improve the linearity of the transconductor, transistors are forced to operate in weak inversion resulting in average power consumption of the proposed OTA to be just 4.45μW.

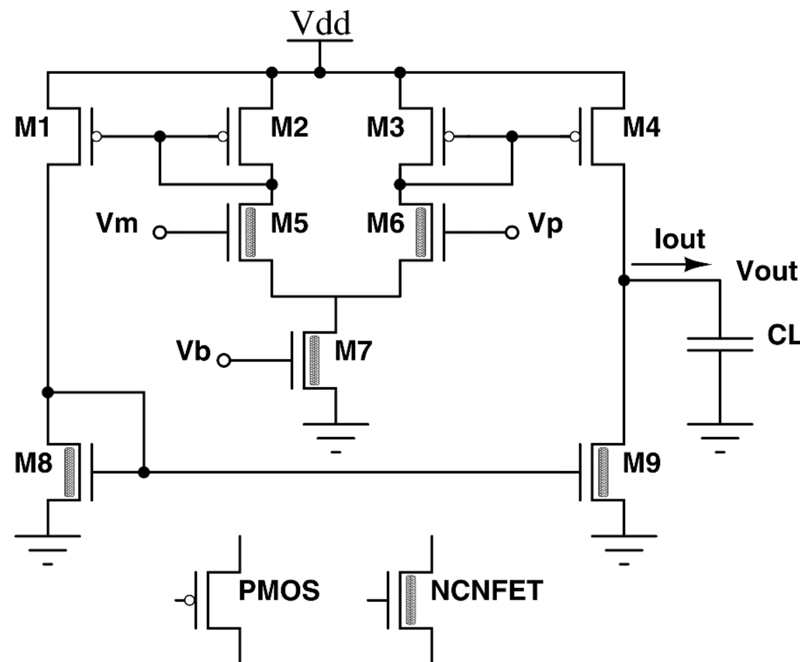


Fig. 4.2 Hybrid transconductor

4.4 Hybrid OTA-C Filters

Utilizing the hybrid transconductor shown in Fig. 4.2 different filter structures such as 1st order (Fig. 4.4), 2nd order (Fig. 4.6), 5th order elliptic low pass (Fig. 4.10) and 2nd order notch (Fig. 4.6) OTA-C filter structures are realized and simulated with HSPICE simulation tool. The 2nd order filter structure shown in Fig. 4.6 is a configurable filter structure with different configurations such as low pass, high pass, band pass and band reject (notch) circuits. Filtering along with low noise amplification is an important signal conditioning requirement of the typical biomedical signal processing chain. For most of the biomedical applications typical frequencies (cut off) of interest fall within few hertz to around 150Hz.For example typical patient monitoring filter cutoffs are- respiration-15Hz, EEG (Electro-encephalogram)-35Hz, EOG (Electro-oculogram)-35Hz, ECG (Electrocardiogram)-70Hz, EMG (Electromyogram)-100Hz and snoring-100Hz. The frequency ranges for these physiological signals and their origins are given in [89]. The bandwidth characteristics differ for these physiological signals and typical filter cut off recommendations also vary depending upon the specific application. The diagnostic requirement of low pass filter cutoffs is different with recommendations as 15Hz for ECG, 70Hz for EEG and 500Hz for EMG. Design of very low-frequency filters for these applications has been a major concern due to the requirement of large valued passive components [90]. To achieve low cutoffs using OTA-C filters need large capacitors. Realizing large value capacitance/area using conventional CMOS technology poses several issues such as area overhead and parasitic effects. Even a gate channel capacitor approach which can offer considerably large capacitance/area has a limitation that the voltage across it should be larger than the threshold voltage. This issue can be tackled with a usage of VLSI-MOS compatible deep trench

capacitors and Integrated Passive Device (IPD) technology. Technological advances such as embedded deep trench capacitors and Integrated Passive Device (IPD) technology has enabled usage of large value capacitors for very low-frequency cutoff filters. Both deep trenching and IPD approach allows integration of high capacitance/area in a monolithic chip [91]–[94]. A wide range of capacitors from pF to μF can be realized in a CMOS high-density deep trench technology. Deep trench capacitors offer benefits over several fronts, first, high-density integration allows close placements giving significant area advantage with minimal parasitic effects, secondly, leakage current is significantly less as compared to conventional MOS capacitors, third, deep trench capacitors exhibit higher quality factor, minimum variability with respect to temperature and higher aspect ratios on account of vertical geometry [95]. Fig. 4.3 shows the cut section of a typical deep trench capacitor. It consists of a vertical trench etched into a Si substrate, a p+ outer region forming one plate, an oxide layer and the inner p+ polysilicon deposition forming another plate of the capacitor. Deep trench capacitors owing to their inherent benefits of high density per unit area, large values and on-chip integration capabilities become suitable candidates for achieving very low cut off frequency for biomedical filters.

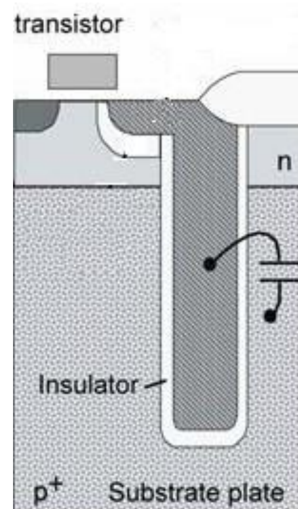


Fig. 4.3 Deep trenching in CMOS process for area efficient large capacitors

4.5 Results and Discussions

First order realization of low pass filter using the hybrid transconductor is shown in Fig. 4.4. Eliminating the need of resistors and inductors this simple filter structure has the transconductance g_m and/or capacitance(C) as the electronic tuning knobs to decide filter cut-off frequency. The transfer function in terms of the transconductance g_m and capacitance C of the first order filter structure is given by equation 4.2.

$$\frac{V_{out}}{V_{in}} = \frac{gm}{sC + gm} \tag{4.2}$$

The desired cut off frequencies can be obtained either by adjusting the value of g_m or by choosing an appropriate value for the capacitor.

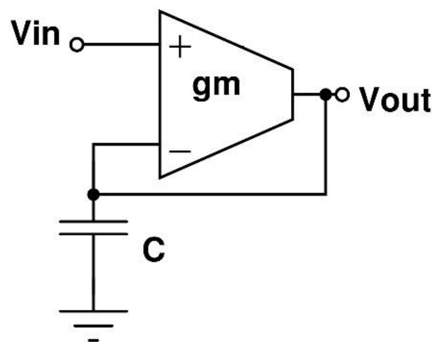


Fig. 4.4 1st order low pass OTA-C filter

The bias current of the transconductor decides the g_m. The bias current is set to 0.1µA by appropriately sizing the transistors. A small value bias current results in very low-frequency cutoffs for the intended application and at the same time reduces power dissipation significantly. Keeping the bias current as low as possible is one of the most efficient ways to reduce power dissipation in OTA-C filters. The proposed filter structures used a fixed transconductance (g_m) and are tuned electronically to achieve desired cut off frequencies by suitably choosing capacitor values.

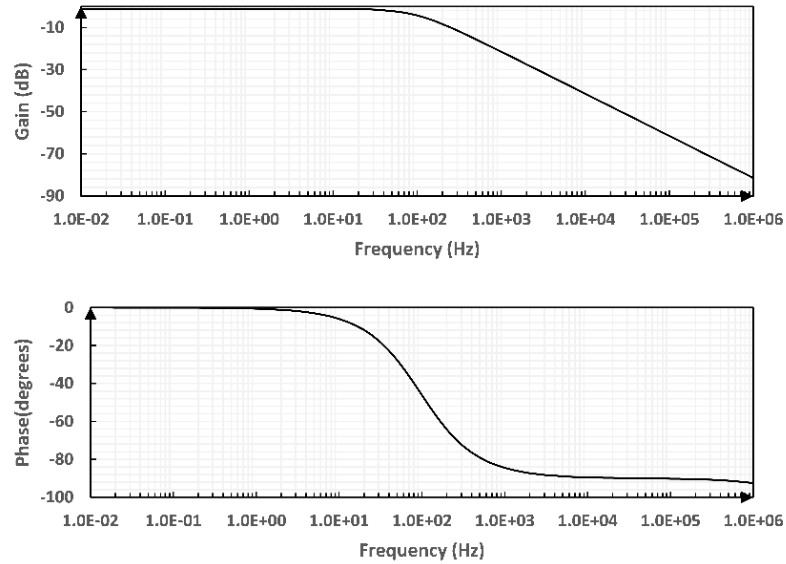


Fig. 4.5 Frequency response of 1st order low pass OTA-C filter

Frequency response showing the magnitude (gain) and phase plots for the first order OTA-C filter are shown in Fig. 4.5. The capacitance selection in the range of 1pF to 10000pF results in 3dB cut off frequency between 300 KHz to 30Hz. For example, a 3000pF capacitor results in low pass 3dB cut off frequency of 100Hz. The average power consumption of the first order low pass filter circuit is 216nW.

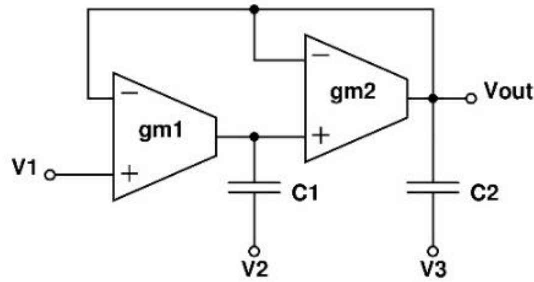


Fig.4.6 2nd order low pass OTA-C filter

Fig. 4.6 shows the configurable filter structure in its second order form (transfer function is given by equation 4.3) and Fig 4.7 gives its frequency response for a low-pass configuration.

$$\frac{V_{out}}{V_{in}} = \frac{gm1gm2}{s^2C1C2 + sC1gm2 + gm1gm2} \tag{4.3}$$

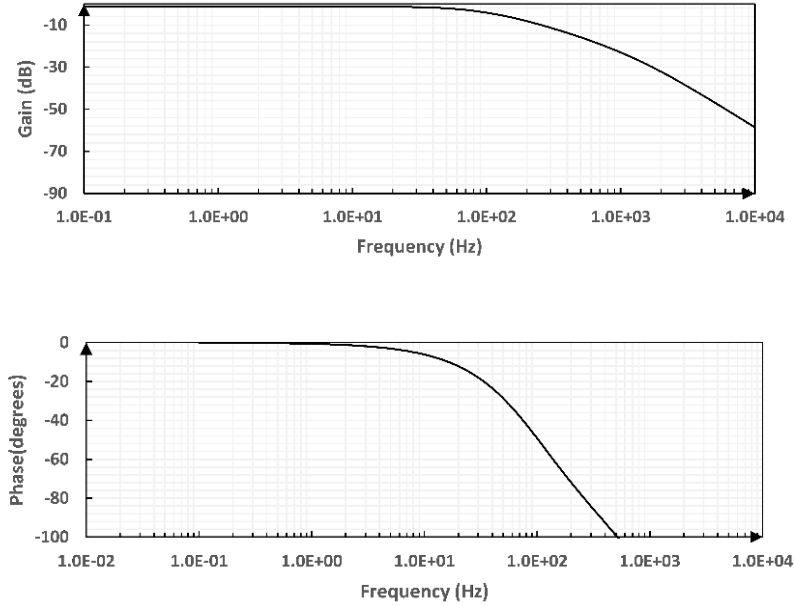


Fig. 4.7 Frequency response of 2nd order low pass OTA-C filter

Different configurations such as low pass, high pass, band pass and band reject (notch) circuits are possible with appropriate inputs. A low pass realization is obtained when we provide an input signal (Vin) at terminal V1 and terminals V2 and V3 are grounded. The output equation of the second order low pass OTA-C filter is given by,

$$V_{out} = \frac{s^2 C1C2V_3 + sC1gm2V_2 + gm1gm2V_1}{s^2 C1C2 + sC1gm2 + gm1gm2} \tag{4.4}$$

For both the OTA's in the filter structure we keep the transconductances gm1 and gm2 equal while desired cut off frequency of 100Hz is obtained by choosing C1=3000pF and C2=200pF. Similarly to obtain lower cut off frequency of 30Hz, C1=500pF and C2=10000pF are used. C1=50pF and C2=4000pF are chosen to obtain 70Hz cutoff. A 433nW power is consumed by this circuit. The second order filter of Fig. 4.6 is configured as 50Hz notch filter by applying input signal (Vin) to terminals V1 and V3 and grounding the terminal V2 with capacitance values of C1=10000pF and C2=3100pF. A 50Hz interference is a standout amongst the most

undesired factors amid ECG signal processing. The weak bioelectric signal becomes easily susceptible and can be contaminated by the 50Hz noise entering the analog front ends through capacitive couplings, leads wires, electrodes as well as from the electrical gadgets in the vicinity [96]. One cannot neglect 50Hz/60Hz power line frequency noise in case of biopotential measurements and hence a notch filter is an essential requirement in biomedical signal processing [97]. In case the 50Hz interference falls within the band of the physiological signal of interest, utmost care has to be taken to design a notch filter with a good Q-factor. For example, a 50Hz notch filter with a poor Q-factor will defeat the purpose of having good ECG filtering, because it will distort the original ECG profile (signal of interest) which falls within the same frequency band. The frequency response showing a 50Hz rejection is given in Fig. 4.8 and the notch circuit consumes 431nW power.

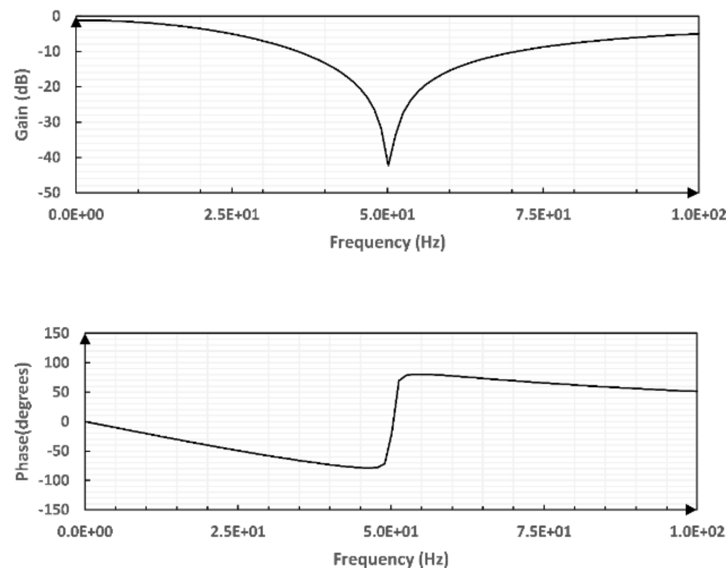


Fig. 4.8 Frequency response of OTA-C notch (50Hz) filter

A low cut off (10Hz) high pass version can be realized with Fig. 4.6 by grounding terminals V1, V2 and applying input signal (Vin) to terminal V3. The frequency response of the high pass OTA-C filter is shown in Fig. 4.9 and the circuit

consumes 45nW power. Such type of very low cut off is essential to eliminate DC and low-frequency components introduced by the skin-electrode interface in the physiological measurements. For example, a surface EMG signal is often contaminated by the noise introduced at the skin-electrode interface due to muscle movements and electrochemical noise. Typical high pass filter cut off recommendations for this application range from 5Hz to 20Hz [98].

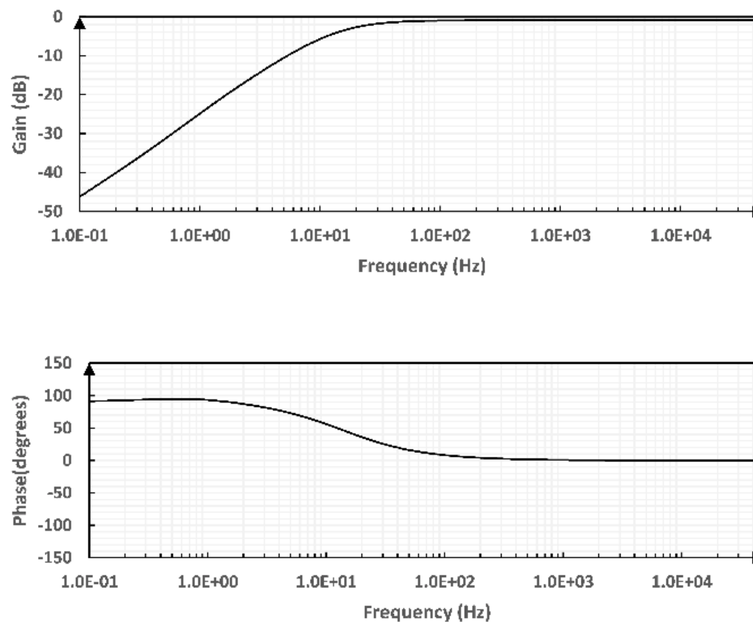


Fig. 4.9 Frequency response of OTA-C high pass filter

A more complex hybrid OTA-C filter realization is a fifth order elliptic structure exhibiting sharper roll-off is shown in Fig. 4.10. The faster transition from pass band to stop band or sharper roll-off is characterized by ripples in the passband as well as in stop band. Elliptic filters are characterized by highest nonlinear phase response as compared to the other classical filter structures. However, they are the preferred choice for obtaining desired magnitude response at the minimal filter order. The proposed elliptic filter dissipates 1.4714μW power. The frequency response (Fig. 4.11) with 100Hz cut off is obtained with capacitances C1-C5 equal to 2000pF, C6=2500pF and C7=1000pF.

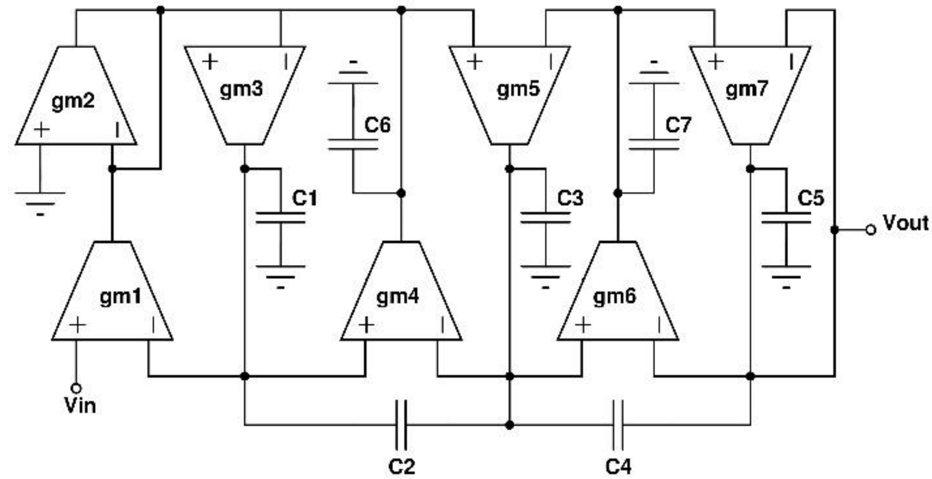


Fig. 4.10 5th order elliptic low pass filter

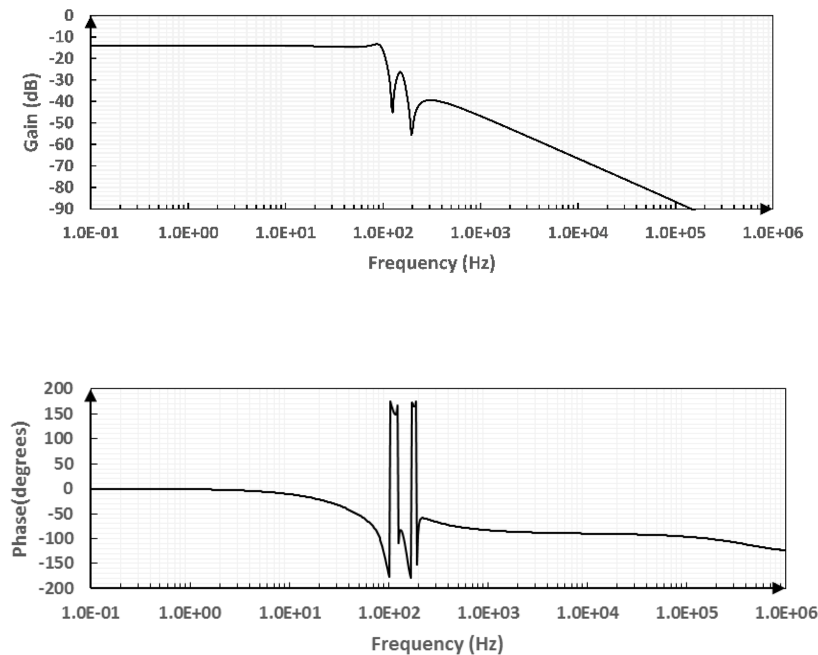


Fig. 4.11 Frequency response of 5th order elliptic low pass filter

In this chapter, we have presented the application of proposed filter structures for different filtering needs in complex and very low frequency physiological or biomedical signals. Performance comparison for the 2nd order and 5th order filters have been given in Table 4.1. Noise removal with respect to 50Hz power line frequency noise (notch filter) and skin-electrode interface noise removal using a

high pass filter is also discussed. However one needs to explore further and investigate filter designs that deals with different kinds of noise signals such as baseline wander, motion artifacts, noise due to muscle contractions and the internal noise generated by the signal processing circuit itself.

Table 4.1. Performance comparison of filter structures

Parameter	[99]	[100]	[101]	This Work	[102]	[96]	This Work
Supply Voltage	1.25V	3.3V	3.3V	0.9V	1V	± 1.5V	0.9V
Filter Order	2	2	2	2	5	5	5
Bandwidth	750Hz	15Hz	50Hz	100Hz	250Hz	37Hz	100Hz
Power	2.5μW	1μW	1.2μW	433nW	453nW	11μW	1.47μW
Power per pole	1.25μW	0.5μW	0.6μW	216nW	90.6nW	2.2μW	0.294μW

4.6 Summary

OTA-C filters for biomedical signal processing, designed with hybrid CMOS-CNFET operational transconductance amplifier as a building block has been presented in this chapter. CNFETs are proposed as an alternative to silicon MOSFET, but in near future, it is very difficult to replace the CMOS technology because of research advancement and economic impact of CMOS based devices. To bridge the gap CNFET technology can be combined with proven CMOS technology resulting in hybrid CMOS-CNFET circuits which can form the basis of a variety of circuits and systems. Owing to difficulties in realizing the required large value capacitors in CMOS process one can opt for integrated deep trenching or integrated passive device technology for the proposed filters. In addition to capacitance and transconductance variation, desired cutoffs can also be achieved by choosing the appropriate number of nanotubes.

Chapter 5

HYBRID VOLTAGE REFERENCE CIRCUITS

5.1 Introduction

This chapter describes, (i) A novel hybrid CMOS-CNFET bandgap reference circuit consisting of a CMOS bandgap core and a CNFET error amplifier, and (ii) A dual threshold voltage reference circuit. The hybrid bandgap reference uses both CMOS and CNFET circuits based on 32nm technology node. Resulting hybrid topology utilizes resistive subdivision method and low threshold CNFET devices to lower the common mode input voltage of the error amplifier. The proposed bandgap reference achieves temperature coefficient of 6.8 ppm/°C at 1.4V power supply over the temperature range of -25°C to 125°C. The circuit produces a reference voltage of around 500mV with line sensitivity of 0.74 %/V and dissipates 26µW power. Another circuit presented in this chapter, the dual threshold voltage reference circuit, exploits subthreshold conduction and V_{th} difference between two CNFETs to achieve ULP consumption of just 3.42pW. This chapter is organized as follows. Section 5.2 covers reference voltage sources and takes a review of various reference voltage circuits. The two different circuits are described in section 5.3 and section 5.5. Results and discussion are given separately for the two circuits in section 5.4 and section 5.6 respectively.

5.2 Reference Voltage Sources

Reference voltage sources are circuits that should provide a dc voltage signal which is highly stable and precise, insensitive to temperature and power supply variations. A good voltage reference circuit possesses thermal stability and high power-supply rejection. Bandgap reference circuit is the one which satisfies this

requirement and hence is an essential component required in many analog, digital and mixed-signal systems such as voltage regulators, ADC's, DAC's, radio frequency (RF) systems and data acquisition systems [103]–[105]. A typical bandgap reference circuit is characterized by different performance metrics such as effective temperature coefficient (TC_{eff}), minimum supply voltage (V_{ddmin}), power consumption, line sensitivity (LS), power supply rejection ratio (PSRR) and silicon area. The expressions for these important performance metrics is given as,

$$TC_{eff} = \frac{V_{ref_max} - V_{ref_min}}{\Delta T\left(V_{ref_nom}\right)} \tag{5.1}$$

$$LS = \frac{V_{ref_max} - V_{ref_min}}{\Delta V_{dd}} \tag{5.2}$$

$$PSRR(jw) = \frac{V_{ref(jw)}}{V_{dd(jw)}} \tag{5.3}$$

Most of the traditional bandgap references rely on long channel designs to reduce the impact of temperature and process variations. This is because scaling does not provide significant benefits in analog circuit designs such as bandgap references due to non-idealities such as short channel effects and gate leakage [106], [107]. Therefore with the aggressive scaling, it has become more difficult to design precise bandgap references in the nanometer regime. In this chapter, we propose a hybrid bandgap reference in a 32nm technology node incorporating a CMOS bandgap circuit with a CNFET based error amplifier.

The first prototype system for a silicon bandgap reference voltage source was proposed by Hilbiber in [108]. He proposed a technique that compensated first order temperature dependence of the base to emitter voltage with a simple circuit that used two different types of diodes. Widlar et al. [109] proposed a new topology of the bandgap reference. This circuit required lower supply voltage and used a technique

that adds the base to emitter voltage with a differential base to emitter voltage of two transistors possessing different current densities. Kuijk et al.[110] developed bandgap reference which used the same principle as that of [108]. In his circuit output voltages, other than the bandgap voltage, could also be realized. Brokaw et. al. [111] presented a bandgap reference which, combined methods reported in [108] and [109]. A switched capacitor bandgap reference employing curvature correction was proposed by Song et.al. [112]. Vittoz et. al. [113] published a CMOS bandgap reference. Banba et.al. [114] proposed a sub-1-V CMOS bandgap reference circuit, with a minimum supply voltage of 0.84V. Leung et. al. in [115] proposed a modified version of the Banba reference[114]. This circuit uses a pMOS input stage in the error amplifier and the inputs of the error amplifier are received after the resistive division. The curvature problem in the bandgap reference can be dealt with different curvature compensation techniques as reported in [103]–[106]. The proposed bandgap reference achieves hybridization of CMOS with emerging CNFET technology in a complementary manner.

5.3 Hybrid Bandgap Reference utilizing CNFET Error Amplifier

The proposed bandgap reference uses hybridization of conventional CMOS technology with carbon nanotube field effect transistors (CNFETs). The basic bandgap itself is a kind of hybrid circuit wherein parasitic BJTs are used out of CMOS technology. The proposed reference uses three conventional PMOS transistors, parasitic BJTs and error amplifier which is a differential amplifier utilizing CNFETs. Bandgap reference works on a principal of cancelling the negative temperature dependence of a p-n Junction with a positive temperature dependence circuit [110], [115] The voltage across the base-emitter V_{BE} of bipolar junction transistor (BJT) has a negative temperature coefficient of about -2mV /° C.

The thermal voltage V_T has a positive temperature coefficient of 0.086mV / °C is multiplied by a constant, which is proportional to absolute temperature. Since p-n junction V_{BE} decreases approximately linear with temperature while V_T increases linearly with temperature. A temperature independent reference can be obtained by multiplying V_T by a constant and summing it with V_{BE}. This concept can be realized with the current mode bandgap reference circuit [115] as shown in Fig 5.2. The required current that becomes proportional to absolute temperature (P_{TAT}) can be suitably obtained as illustrated in Fig. 5.1.

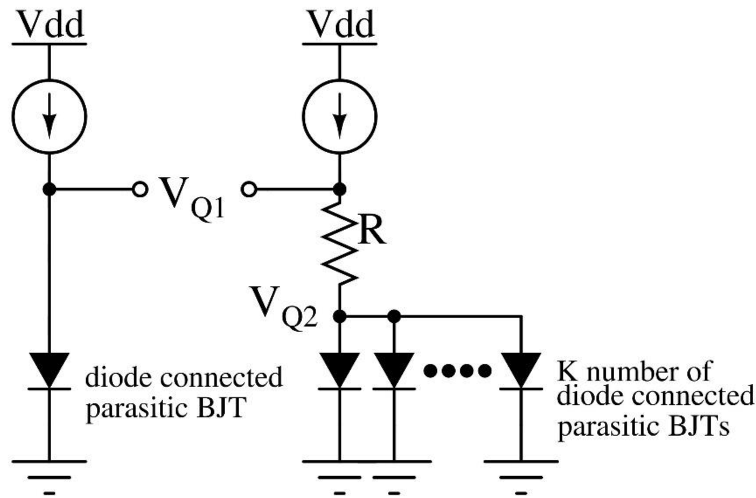


Fig. 5.1 Generating a current proportional to absolute temperature

Considering diode equations 5.5 and 5.6, we can derive the expression for P_{TAT} current. As shown in Fig. 5.1, the node voltage V_{Q1} and the voltage at the junction of the current source and the resistor forms a differential input, being given to the very high impedance nodes of CNFET error amplifier (Fig. 5.3). So we can write,

$$V_{Q1} = V_{Q2} + I_{Q2}.\, R \tag{5.4}$$

$$V_{Q1} = n\,.V_T.\, ln\, \frac{I_{Q1}}{I_s} \tag{5.5}$$

$$V_{Q2} = n\,.V_T.\, ln\, \frac{I_{Q2}}{K.\, I_s} \tag{5.6}$$

$$V_{Q1} - V_{Q2} = n.V_T.\ ln\frac{I_{Q1}}{I_s} - n.V_T.\ ln\frac{I_{Q2}}{K.\ I_s} \tag{5.7}$$

$$I_{Q2}.\ R = n\,V_T\left(ln\frac{I_{Q1}}{I_s} - ln\frac{I_{Q2}}{K.I_s}\right) \tag{5.8}$$

$$I_{Q2}.\ R = n\,V_T\ \ ln\frac{I_{Q1}/I_s}{I_{Q2}/K.\ I_s} \tag{5.9}$$

$$I_{Q2}.R = n\ .\ V_T\ .\ ln\,K \tag{5.10}$$

Current through both the branches being equal ie- $I_{D1}=I_{D2}=I=I_{PTAT}$, the I_{PTAT} expression becomes,

$$I_{PTAT} = I = \frac{n.\ V_T\ ln\,K}{R} \tag{5.11}$$

Similarly, the I_{CTAT} current expression can be written as,

$$I_{CTAT} = \frac{V_{Q1}}{L\,R} \tag{5.12}$$

Summing the two current expressions and rewriting the expression in terms of V_{ref} we obtain,

$$V_{ref} = \left(\frac{n\,V_T\,N\,ln\,K}{R} + \frac{V_{Q1}}{L\,R}\right)NR \tag{5.13}$$

$$V_{ref} = n\,V_T\,N\,ln\,K + \frac{N}{L}\,V_{Q1} \tag{5.14}$$

$$\frac{\partial Vref}{\partial T} = n.\ N.ln\,K\ .\ \frac{\partial V_T}{\partial T} + \frac{N}{L}\ .\ \frac{\partial V_{Q1}}{\partial T} \tag{5.15}$$

$$\frac{\partial V_T}{\partial T} = 0.085mV/C\ and\ \frac{\partial V_{Q1}}{\partial T} = -1.6mV/C$$

$$for\ zero\ TC\ ,\ \ L = \frac{1.6}{n.ln\,K\ .\ 0.085} \tag{5.16}$$

$$N = \frac{V_{ref}}{n.\ V_T.ln\,K + \frac{V_{Q1}}{L}} \tag{5.17}$$

$R_3 = N.\, R\ and\ R_1 +\ R_2 = L.\, R$

The voltages at nodes A and B are forced to be equal and are given by equation (5.18). The reference voltage V_{ref} across the resistor R3 is given by equation (5.19).

$$V_A = V_B = \left(\frac{R_2}{R_1 + R_2}\right) V_{Q1} \tag{5.18}$$

$$V_{ref} = \left[\frac{R_3}{R_1 + R_2}\right]\left[\left(\frac{R_1 + R_2}{R}\right) \ln(K)\, V_T + V_{Q1}\right] \tag{5.19}$$

The term V_{Q1} (V_{BE} of the transistor) in the equation (5.18) has a negative temperature coefficient, the second term $\ln(K).V_T$ has a positive temperature coefficient. The K=8 is found to be optimum for our hybrid circuit.

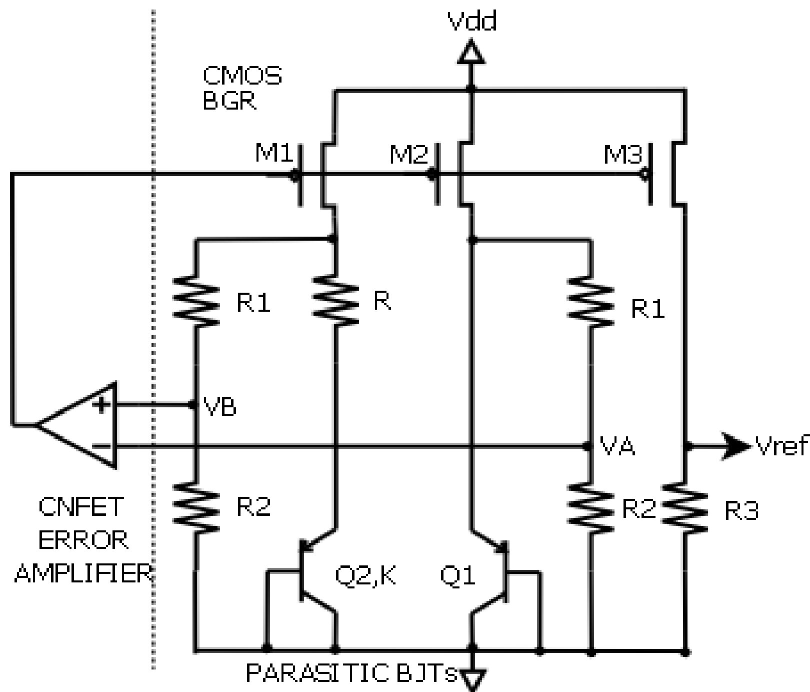


Fig. 5.2 CMOS-CNFET hybrid bandgap reference

A reference voltage with theoretically zero temperature coefficient can thus be obtained by selecting proper value for the resistor ratio. The optimum value of the resistor ratio is obtained by choosing R1=150KΩ, R2=320KΩ, R3=165KΩ and R=40KΩ. Equally sized PMOS devices (W/L=10) operating in the saturation region with their gates tied together results in a current mirror connection. Since the

currents flowing through all the three PMOS devices are equal and are temperature independent, a reference voltage (V_{ref}) across the resistance is also temperature independent.

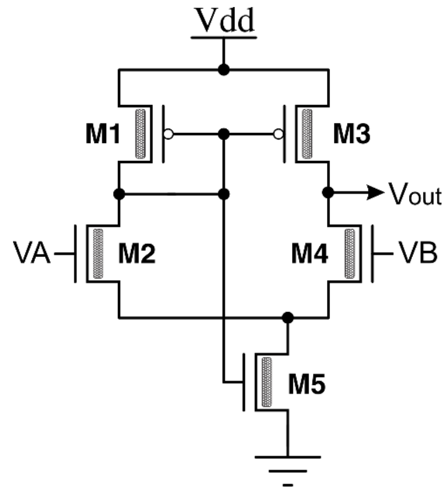


Fig. 5.3 CNFET based error amplifier used in bandgap reference circuit

Fig. 5.3 shows the CNFET based error amplifier used in the bandgap reference. This circuit is a differential amplifier and does not need a separate biasing circuit to set the currents. The two voltage dividers in the bandgap core provide the differential input between input nodes VA and VB. Ideally, VA is supposed to be equal to VB, but practically there is always a mismatch and VA≠ VB. The difference VA-VB called an error voltage is amplified by the error amplifier. This error amplifier must satisfy a condition that its common mode input voltage should not fall below a voltage drop across a single diode. This can be achieved using low-threshold devices as reported in [114] and with transistors in weak inversion [116], as well as with BiCMOS technologies [117]. This work presents a resistive division method to lower the common mode input voltage of the error amplifier which uses low threshold CNFETs. CNFETs with tube chirality (19,0), the number of tubes=3 have been used.

The HSPICE simulations are carried out to determine the performance metrics of the voltage reference such as line sensitivity, temperature coefficient, and a power

supply rejection ratio (PSRR). A wide temperature variation between -25°C to 125°C and V_{dd} sweep of 0 to 2V is chosen. Stanford University carbon nanotube field effect transistors (CNFET) HSPICE model [38], [59] is used to simulate the proposed hybrid circuit.

5.4 Results and Discussion (Bandgap Reference)

5.4.1 Power Supply Dependence(Line Sensitivity)

Fig. 5.4 shows the reference voltage variation, as the supply voltage is swept between 0V to 2.0V. Line sensitivity is an important performance metric governing the stability of the voltage reference with respect to variations in supply voltage. The legends show different operating temperatures at which simulation is carried out. Fig. 5.5 depicts a close-up/magnified view for supply voltage between 1.2V to 1.6V. Simulation results show that the reference has got excellent temperature independence for the V_{dd} around 1.4V. Mean reference voltage is about 500.5mV and changes by +1mV to -2.7mV when V_{dd} is varied from 1.1V to 1.6V. The line sensitivity achieved by the reference is 0.74%/V.

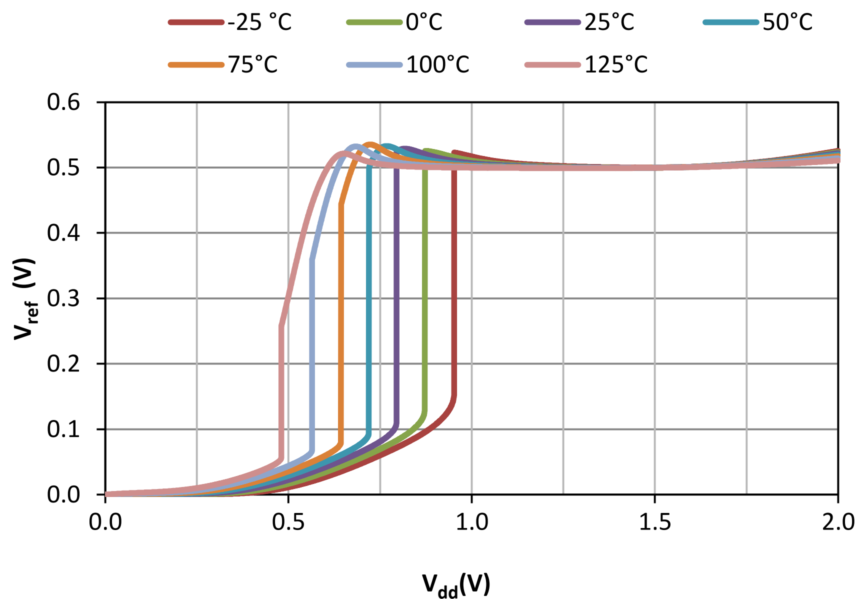


Fig. 5.4 Reference voltage variation for V_{dd} sweep of 0V to 2.0V

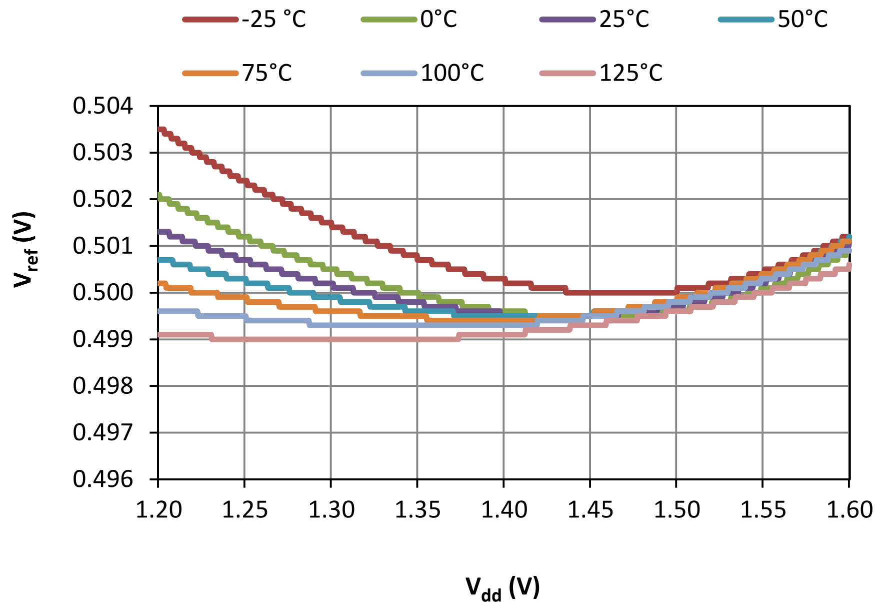


Fig. 5.5 A close-up/magnified view for variation in reference voltage for V_{dd} between 1.2 V to 1.6 V

5.4.2 Temperature Dependence of the Bandgap Reference

A true temperature independent reference cancels a positive temperature coefficient with a negative temperature coefficient. Bandgap reference circuit generates a voltage that is a linear function of temperature and voltage that is complementary to the absolute temperature which is nonlinear because of inherent nonlinearity in a p-n junction diode. Therefore a linear voltage can't be perfectly canceled by the nonlinear voltage. This causes a curvature in the bandgap voltage and is called curvature problem [103], [106]. Fig. 5.5 which shows a close-up view for V_{dd} between 1.2V to 1.6V depicts such curvature. The curvature can be compensated up to certain extent but cannot be eliminated totally and hence practical bandgap references exhibit small but finite temperature dependence. To quantify temperature dependence, effective temperature coefficient is calculated using equation 5.1. Temperature dependence of the bandgap reference for different supply voltages is shown in Fig. 5.6. The temperature coefficient achieved by our

circuit is 6.8 ppm/°C, at a supply voltage of 1.4V and 5.3ppm/°C at 1.5V. A temperature coefficient is 8ppm/°C for 1.6V and degrades to 33ppm/°C for 1.3V.

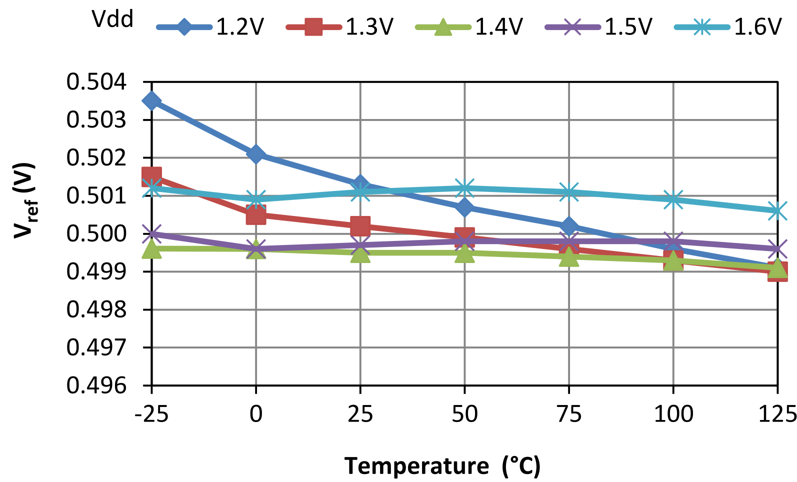


Fig. 5.6 Temperature dependence of the circuit

5.4.3 Power Supply Rejection Ratio (PSRR)

Apart from good temperature independence, it is also expected that a bandgap reference circuit provides high power supply rejection ratio (PSRR) over a wide frequency range. A high PSRR ensures the ability to reject noise. The PSSR performance of the bandgap reference is shown in Fig. 5.7. The circuit exhibits a PSRR of -44dB at 10 KHz frequency, 25°C temperature and for V_{dd} of 1.4V. Similarly, PSRR is of -38dB at the 10MHz frequency.

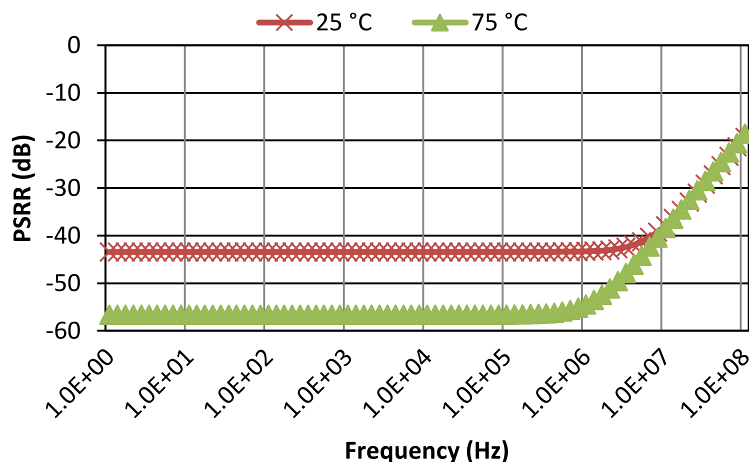


Fig. 5.7 PSRR at 25°C and 75°C, V_{dd}=1.4V

5.4.4 Stability Analysis

Fig. 5.8 and Fig. 5.9 show transient analysis of the proposed circuit. The output voltage settles to 500mV within 240nS with a maximum overshoot of 7mV at 25°C.

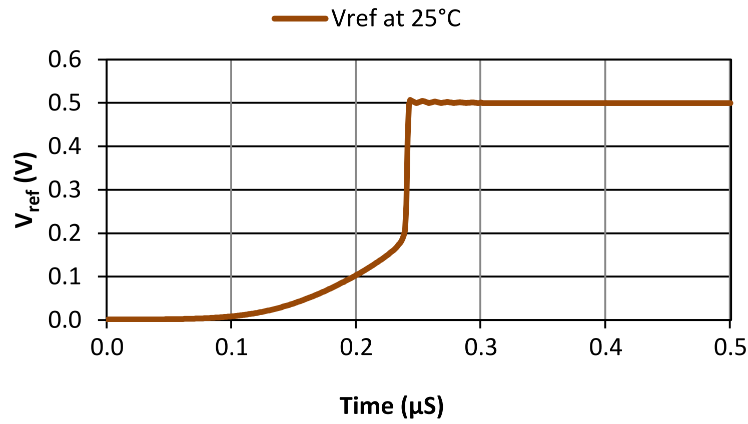


Fig. 5.8 Stability / Transient analysis

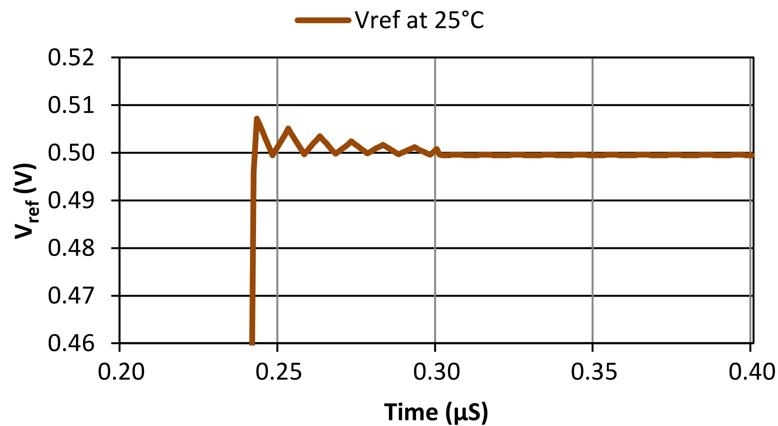


Fig. 5.9 A close-up of transient analysis

Table 5.1. Performance comparison of bandgap reference w.r.t. performance metrics

Parameter	[104]	[118]	[119]	[103]	This Work
Supply Voltage(V)	2.5	1.2	0.9	1.2	1.4
Power Dissipation(µW)	95	48	36	43	26
Ref. Voltage (mV)	617.7	487.6	670	767	500.5
TC (ppm/°C)	3.9	8.9	20	4.5	6.8
Temperature Range(°C)	-15 to 150	0 to 80	0 to 80	-40 to 120	-25 to 125
Line Regulation (%/V)	0.039	0.24	0.27	0.054	0.74

The overall performance comparison of the hybrid bandgap reference with respect to various performance metrics is given in table 5.1.

5.5 Dual Threshold Voltage Reference Circuit

This section presents a voltage reference circuit that exploits subthreshold conduction and threshold voltage difference between two carbon nanotube field effect transistors (CNFETs) to achieve ultra-low power consumption. The circuit produces a reference voltage of 203mV at 0.5V supply voltage, consumes only 3.42pW power and exhibits excellent temperature and power supply independence. The robustness of the proposed circuit for variations in carbon nanotube (CNT) diameter and inter CNT pitch variations is also presented with Monte Carlo simulations.

There is an increasing demand for precision voltage reference circuits which satisfy stringent requirement of ultra-low power consumption along with the process, voltage and temperature tolerance [119], [120]. Many of the modern electronic circuits and systems such as radio frequency (RF) systems, wearable, and implantable sensor systems, and portable/handheld electronic systems find voltage reference as an essential building block [103]. Precision and ultra-low power voltage references have recently become important constituents of the Internet of Things (IoT) devices consisting of battery-powered sensors, actuators and networked intelligence.

For applications in portable/handheld, wearable and implantable devices, the importance of power consumption is significantly elevated. Since these applications are mostly battery powered, low power consumption is critical to extend battery life [1], [71]. Therefore, ultra-low power consumption is of prime importance in the design of the reference voltage. In this section, we present a voltage reference that

satisfies the ultra-low power requirement of portable applications. The proposed voltage reference utilizes just two CNFETs, does not need resistors, and provides excellent temperature stability and power supply rejection. The proposed voltage reference is also investigated for its robustness against CNT diameter and inter CNT pitch variations.

The most common type of voltage reference is the bandgap reference circuit. To decrease the effect of temperature and process variations, long channel designs have been preferred. Also due to short channel effects and gate leakage, there are limits for achieving significant benefits due to scaling in case of analog circuits such as bandgap references [106]. Therefore in a nanometer device regime with aggressive scaling, a design of precise bandgap reference has become a challenging task. Traditional bandgap references use an amplifier for error correction. Incorporation of amplifiers in voltage references results in improved temperature and supply voltage insensitivity [107]. The designs that avoid amplifiers often rely on transistors operating in the saturation region, resulting in a significant power dissipation. The transistors operating in the saturation region require sufficient headroom between supply and threshold voltage, limiting minimum functional V_{dd} [121], [122]. Among the different approaches, the subthreshold design is the most promising approach for ultra-low power applications. In this section, we present a hybrid dual threshold CNFET based voltage reference, wherein transistors operate in the subthreshold region.

The threshold voltage of the intrinsic CNT channel can be approximated to be $V_{th} \approx 0.5/D_{CNT}$ or in terms of the bandgap, we can write equation 5.21. This approximation based on ballistic theory computations is in strong agreement with experimentally extracted value for the threshold voltage. Moreover, the threshold

voltage in case of CNFETs having intrinsic channels is not based on the concept of channel inversion but rather, it is the gate voltage corresponding to maxima of transconductance when we plot $\partial g_m/\partial V_G vs\ V_G$[31]. As per equation 5.20, the tubes with smaller diameters have a larger bandgap, and tubes with larger diameters have a smaller bandgap. There is an inverse dependence of the threshold voltage on tube diameter.

$$E_g \propto \frac{0.8eV}{D_{CNT}} \tag{5.20}$$

$$V_{th} = \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a\ V_\pi}{eD_{CNT}} \tag{5.21}$$

Where E_g is the CNT bandgap, a = 0.246nm is the graphene lattice constant, $V\pi$ = 3.033 eV is the carbon π-π bond energy. V_{th} of CNFET can be controlled by altering the chirality indices or the CNT diameter (expression for D_{CNT} given in equation 1.2). As the chirality indices changes, the V_{th} of the CNFET will also change. CNFET threshold voltages can be approximated either by solving equation 5.21 or can also be obtained by linearly extrapolating I_{DS} vs V_{GS} curves as reported in [123].

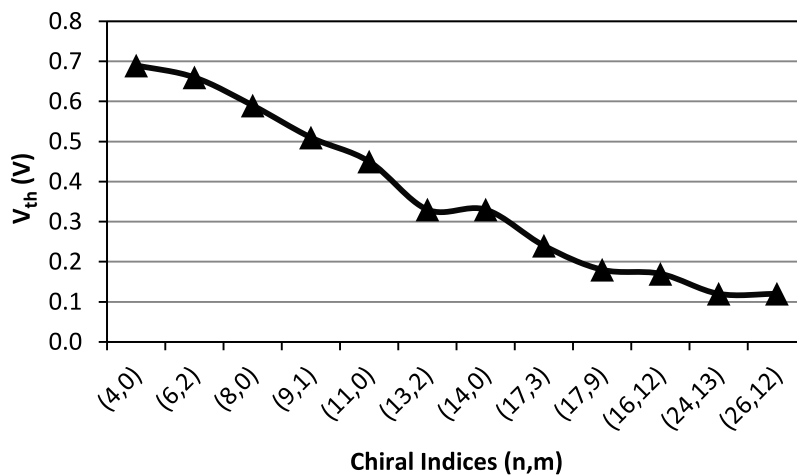


Fig. 5.10 Threshold voltage as a function of chiral indices

Threshold voltages for different combinations of semiconducting chiral vectors is reported in [55], for example, chiral vectors (4,0), (11,0) and (14,0) gives threshold voltages 0.69V,0.45V and 0.33V respectively. Fig. 5.10 shows the threshold voltage plotted against the various combinations of chiral indices.

The proposed circuit utilizing a combination of low V_{th} (0.12V) device and high V_{th} (0.51V) device operating in a subthreshold region is shown in Fig. 5.11. The subthreshold operation allows extremely low levels of supply voltages and ensures ultra-low power consumption for voltage references [121], [122]. Voltage references employing conventional CMOS technology with transistors having different threshold voltages are reported in [121], [122]. In this work, we propose a dual diameter, dual threshold CNFET based voltage reference. A reference voltage of 203mV is achieved with 3.4145pW of power consumption. A compact spice model for CNFETs proposed in [38], [59] has been used and the circuit is simulated with HSPICE software.

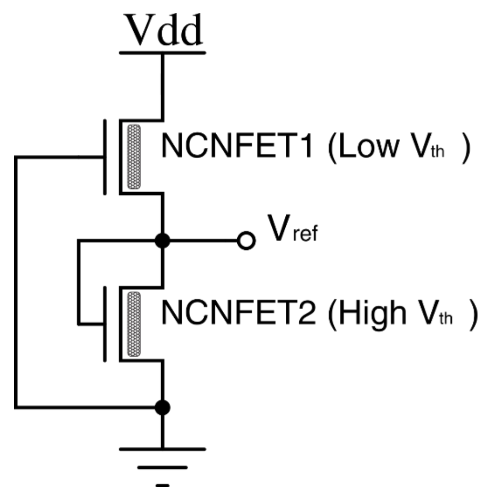


Fig. 5.11 A dual threshold CNFET voltage reference circuit

The upper transistor NCNFET1 as shown in Fig. 5.11 with its gate tied to the ground consists of 3 nanotubes with chiral indices (24, 13). This results in a low V_{th} of 0.12V. Relatively higher V_{th} of 0.51V is used for the lower transistor NCNFET2

with chiral indices (9, 1). Both the CNFETs operate in subthreshold region drawing extremely low drain to source current. The simple expression of the drain to source current I_{DS} of CNFET is given by the equation 5.22.

$$I_{DS} = n\, g_{CNT}\, (V_{DD} - V_S - V_{th}) \tag{5.22}$$

where g_{CNT} is the transconductance of the CNFET, n is number of CNTs in a CNFET, V_S is the voltage drop between an inner and external source node of the transistor and V_{th} is the device threshold voltage.

5.6 Results and Discussions (Dual Threshold Voltage Reference)

To achieve a voltage reference that is insensitive to process variations such as threshold voltage an optimum value of V_{th} difference is to be maintained between the upper and lower transistor. To determine the minimum required V_{th} difference, the proposed circuit is simulated using HSPICE under different combinations of chiral vectors. As per CNT diameter expression and equation 5.21, different chiral vectors gives different CNT diameters, which further results in different threshold voltages for the two transistors. For example an upper transistor with n=24, m=13 results in a V_{th} of 0.12V and n=9, m=1 results in V_{th} of 0.51V giving a net V_{th} difference of 0.39V. Fig. 5.12 shows reference voltage and reference current as a function of V_{th} difference between the upper and lower transistor. Similarly, Fig. 5.13 shows reference voltage and average power as a function of V_{th} difference.

As per the simulation results shown in Figure 5.12 and 5.13, for V_{th} difference greater than 0.39V V_{ref} becomes insensitive to the variations in threshold voltages. Any change in the threshold voltage of either of the two transistors will result in variation in reference voltage if the V_{th} difference falls below 0.39V, otherwise, reference voltage will be maintained constant. The upper transistor operates in the subthreshold region while the lower transistor determines the reference current.

Higher the threshold voltage of the lower transistor as compared to the upper transistor, lower is the reference current drawn resulting in an ultra-low-power consumption.

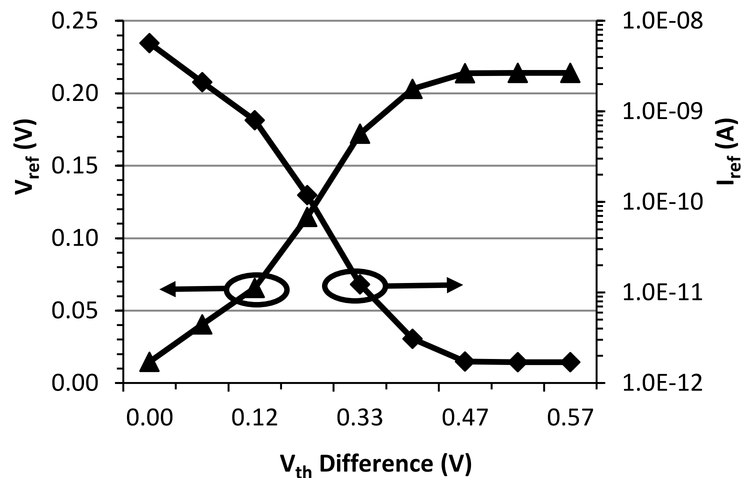


Fig. 5.12 Reference voltage and current as a function of V_{th} difference

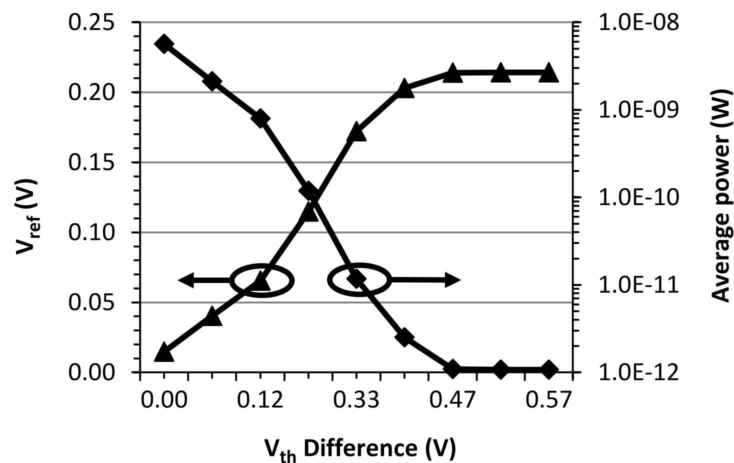


Fig. 5.13 Reference voltage and average power consumption as a function of V_{th} difference

CNFETs offer several benefits over conventional MOSFETs in the subthreshold region and provide superior performance in the subthreshold region. The drain to source current I_{DS} of CNFET in subthreshold region (weak inversion) is significantly greater than that of conventional MOSFET. CNFETs almost does not exhibit non-ideal effects such as gate-induced drain leakage (GIDL) and drain-induced barrier lowering (DIBL). Subthreshold conduction in the CNFETs is mainly because of the

band-band tunneling via the semiconducting sub-bands [38], [59]. The resulting current is referred to as BTBT current I_{btbt}. The drain to source current due to the band to band tunneling depends on threshold voltage V_{th} and also on the number of CNTs in the transistor.

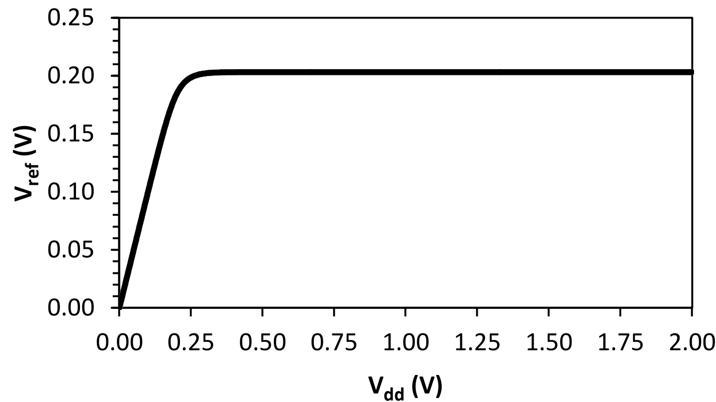


Fig. 5.14 Reference voltage vs V_{dd} (Temperature sweep -25°C to 125°C)

Fig. 5.14 shows the reference voltage generated at the node V_{ref} formed between drain-source of the two CNFETs. The gate of the upper transistor is permanently tied to ground while the reference voltage is applied to the gate of the lower transistor resulting in a cascode configuration which further makes the reference voltage immune to changes in supply voltage. The HSPICE simulations are carried out to test temperature dependence of the reference by varying temperature between -25°C to 125°C (V_{dd} sweep between 0 to 2V). Simulation result shows that the reference has got excellent temperature independence exhibiting near zero temperature coefficient. This is because unlike MOSFETs, in CNFET devices, the influence of temperature on V_{th} is insignificantly small [55]. Simulation results reported in [55] shows a negligible V_{th} variation for the temperature range of -25°C to 125°C. Another remarkable aspect of CNFETs with gate oxide capacitance (C_{ox}) much greater than CNT quantum capacitance (C_q) is the insignificantly small temperature dependence of the CNFET transconductance [31]. For the proposed

voltage reference mean reference voltage is about 203mV for a range of V_{dd} between 0.3V to 2V. The minimum V_{dd} required for the circuit to provide a stable reference voltage is 0.3V.

Many of the on-chip high-speed digital circuits generate noise and hence demand a good power supply rejection ratio (PSRR) over a wide frequency range from the on-chip voltage reference. A good PSRR for a voltage reference indicates its ability to reject ripple or noise in the power supply. The PSSR over the range of frequency for the voltage reference is shown in Fig. 5.15. The circuit exhibits a PSRR of -86dB at 10 KHz frequency, 25° C temperature and for V_{dd} of 0.5V. Similarly, PSRR is of -102dB at the 10MHz frequency. Fig. 5.16 show transient analysis of the proposed circuit. The output voltage settles to 203mV within 0.5µS.

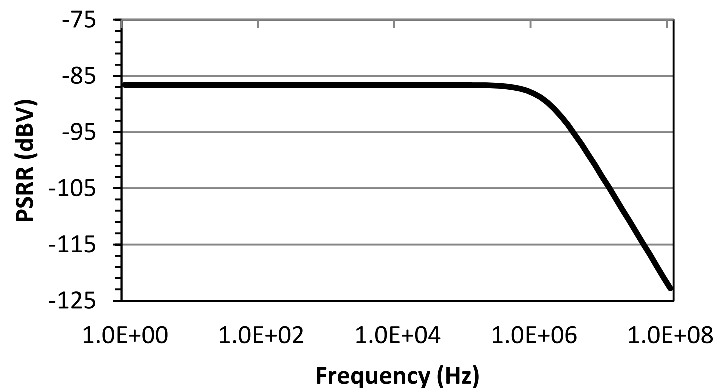


Fig. 5.15 PSRR at 25^0C , V_{dd} = 0.5 V

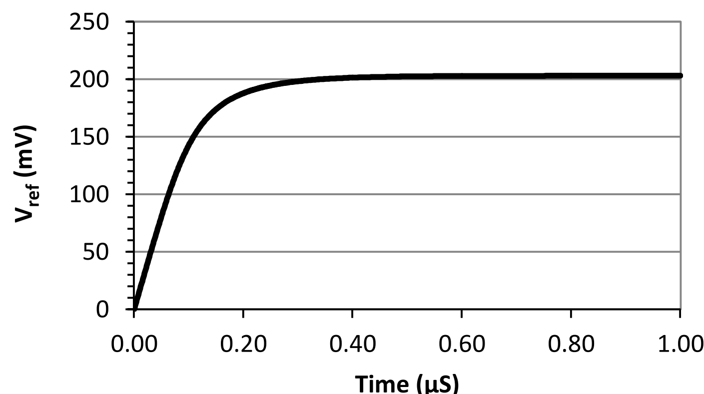


Fig. 5.16 Transient analysis

Performance comparison of the dual threshold voltage reference with the voltage reference of [121] is given in Table 5.2.

Table 5.2. Performance comparison with CMOS dual threshold voltage reference

Technology	Upper Transistor M1	Lower Transistor M2	V_{ref}	Power Dissipation	Temperature Coefficient (TC)
Seok et.al.[121] 130nm CMOS	L=60μ W=3.3μ (native thick oxide ,near zero V_{th})	L=60μ W=1.5μ (High V_{th})	175mV	2.2pW	62 ppm/^{o}C
This work CNFET 32nm	No of tubes =3 Chiral Vector m = 24 n = 13 V_{th0} = 0.12 (Low V_{th})	No of tubes =3 Chiral Vector m=9 n=1 V_{th0} = 0.51 (High V_{th})	203mV	3.4145pW	0 ppm/^{o}C

5.7 Variability Analysis of the Voltage Reference

Just like conventional CMOS, CNFETs are also prone to manufacturing variability and hence one cannot ensure manufacturing of exactly identical CNFETs. This results in device mismatch consisting of random variations in device characteristics which in turn causes behavioral variation from circuit to circuit. Monte Carlo analysis is often used to investigate the effect of such type of variability on the overall circuit performance. In this section, we present the effects of diameter and inter CNT pitch variations on the proposed voltage reference using Monte Carlo simulations. Monte Carlo analysis is a statistical analysis that is used to predict overall circuit behavior under random variations of the device parameters within a specified tolerance. Based on the possible variations in the parameters either a uniform or Gaussian distribution of the inputs are generated to obtain deterministic Monte Carlo simulation output.

5.7.1 Variability Issues in CNT and CNFETs

Although it is desired that one should develop imperfection immune manufacturing process, present CNT growth/synthesis processes pose several difficulties in terms of proper alignment (parallel), improper placement (mis-positioning), inconsistency in obtaining unique diameter, presence of impurities such as metallic CNTs, CNT density variations and doping concentration variations. Fig. 5.17 shows various imperfections in manufactured CNFETs.

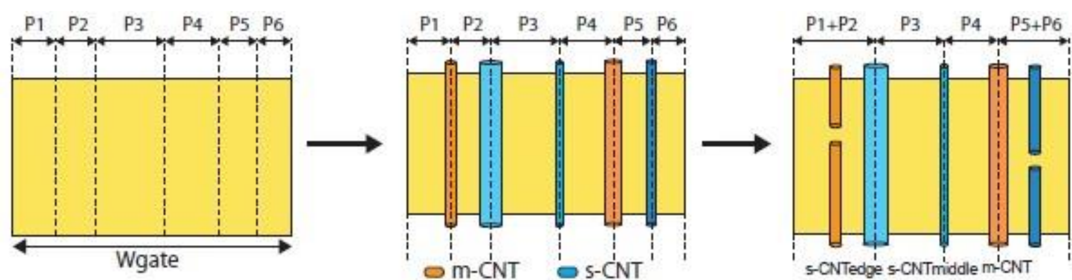


Fig. 5.17 Imperfections in inter CNT pitch, diameter and mixed CNTs

Growth methods that use piezoelectric quartz substrates can produce more than 99.9% perfectly aligned CNTs however one cannot guaranty precise placement of these perfectly aligned CNTs at the desired location. For example, precise placement of the desired number of CNTs exactly beneath the gate of the CNFET still remains a challenge. These kinds of imperfections may not give correct logic behavior of the circuit. This issue has been addressed in [124] by developing an algorithmic (for layout design) and automated technique for making logic circuits immune from misaligned and mis-positioned CNTs.

Other major concerns for CNFET circuits are difficulties such as controlling the diameter of the SWCNT and the percentage of metallic CNTs produced [125]. Different CNT growth techniques such as laser ablation, chemical vapor deposition (CVD), high-pressure carbon monoxide decomposition (HPCO) and arc discharge method are used for the manufacturing of CNTs. However, these techniques produce

a mixture of CNTs with various chirality. Variations in chirality results in diameter variations that affect the drive current and the V_{th} of the CNFETs [126]. Chirality also decides nature of CNTs ie- semiconducting or metallic. Presence of metallic CNTs beneath the gate of manufactured CNFET causes difficulty to turn off the device, increasing leakage because of conducting nature of metallic CNTs, degradation in noise margin in logic circuits and unpredictable circuit behavior. There exist two alternative approaches to ensure the presence of only semiconducting CNTs. The first one tries to synthesize maximum semiconducting CNTs during wafer level growth process [127]. The second approach uses a post process that eliminates metallic CNTs either by self-heating (passing excessive current through them) or by using chemical reagents to remove metallic CNTs [128], [129]. The second approach inadvertently removes a few numbers of semiconducting CNTs as well.

5.7.2 Monte Carlo Analysis for the Effect of Diameter Variability on the Voltage Reference

Based on the manufacturing process of CNTs, various mean diameters and diameter variations are witnessed. Experimental results so far indicate a Gaussian distribution for the diameter of CNTs grown using different growth techniques. These growth techniques have shown that the variability can be reduced to the extent of standard deviation of the CNT diameter being curtailed below 10% of the mean CNT diameter [57], [126]. The Monte Carlo simulation (Fig.5.18) were performed with diameter variation achieved via variations in chirality of both the CNFETs. For the upper CNFET, a Gaussian distribution with nominal chirality of (24,13) and a 3σ variation of 0.5 is considered. For lower CNFET, a Gaussian distribution with

nominal chirality of (9,1) with a 3σ variation of 0.2 is considered. The results of the Monte Carlo analysis gave μ=0.2031, σ = 0.0032 and σ/μ = 1.5807%.

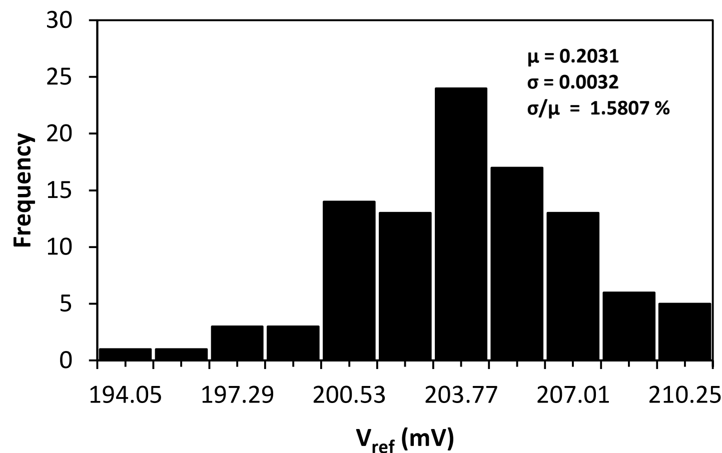


Fig. 5.18 Effect of diameter variability on the reference voltage

5.7.3 Monte Carlo Analysis for the Effect of Inter CNT Pitch Variability on the Voltage Reference

Another challenge in the CNT growth process is the density variation resulting in non-uniform distribution of the grown CNTs in the CNFET channel. The existing fabrication processes do not ensure uniform spacing between adjacently placed parallel tubes. It is also difficult to provide precise control of the locations of individual CNTs and maintaining consistency in the CNT count. Variations in diameter of the individual CNTs and non-uniform spacing between the tubes contribute to producing inter CNT pitch variations. Due to these variabilities, different CNFET devices then exhibit variations in charge screening effect [130]. This variability in charge screening effect results in large variations in CNFET drive current. To investigate the effect of inter CNT pitch variations, Monte Carlo simulations of the proposed voltage reference circuit were performed with 10nm nominal inter CNT pitch and a 3σ variation of 2.5nm. The Monte Carlo analysis results as depicted in Fig. 5.19, gave μ = 0.2028, σ = 0.0001 and σ/μ = 0.0467%,

which signifies robust performance of the proposed voltage reference under CNT pitch variations.

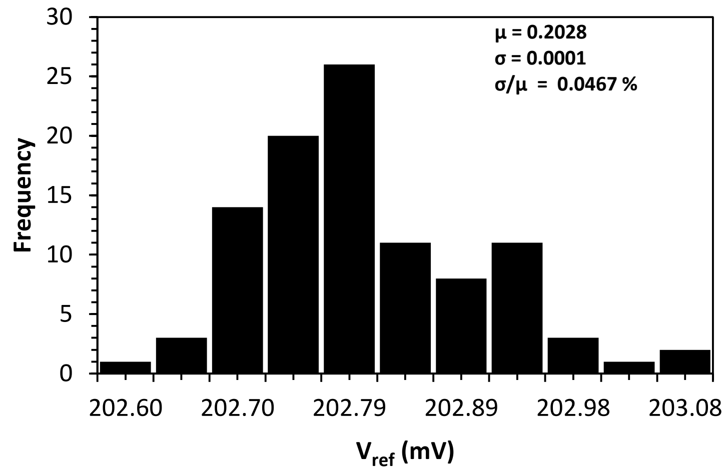


Fig. 5.19 Effect of inter CNT pitch variability on the reference voltage

5.8 Summary

Hybrid CMOS-CNFET bandgap reference has been presented in this chapter. The simulation results confirm the robustness of the reference for variations in temperature and power supply. A precision bandgap reference with a nominal output of 500mV, 6.8 ppm/°C temperature coefficient, 0.74 %/V line sensitivity, and 26μW power dissipation is presented. The circuit exhibits stable operation without compensating capacitors with a startup time of 240nS at 25°C. A PSRR of -44dB is achieved at 25°C for 1.4V power supply. A satisfactory 6.8 ppm/°C temperature coefficient is achieved without any special curvature compensation.

An ultra-low power voltage reference circuit with just two CNFETs having different threshold voltages was also presented. Dependence of reference voltage on the difference between threshold voltages of the CNFET pair arranged in the circuit was investigated. The reference voltage, achieved by the proposed circuit was found to be immune to the V_{th} variations if the V_{th} difference between the CNFET pair was more than 0.39V. Furthermore, the circuit was studied for its temperature

dependence, power supply sensitivity and stability analysis. The circuit exhibited excellent temperature independence, a PSRR of -86dB at 10 KHz, 0.5μS settling time and achieved 203mV reference voltage while consuming only 3.4245pW. Monte Carlo simulations for CNT diameter variation, and inter CNT pitch variations gave σ/μ values 1.5807% and 0.0467% respectively, signifying a robust performance of the circuit.

Chapter 6

CONCLUSION

6.1 Introduction

Apart from architectural and circuit level measures to reduce power consumption one has to pay attention to device level measures and possible hybrid co-integration of CMOS with emerging devices. These new era devices offer massive benefits in terms of aggressive scaling and particularly contribute to a significant area-power reduction in the nanoscale regime. These devices also offer significant avenues for prospective hybrid nano-electronic circuits by means of co-integration with conventional CMOS devices in a complementary manner. Extended CMOS devices having wafer scale manufacturing compatibility with proven CMOS technology have gained significant attention due to their better subthreshold swing that can be achieved as compared to 60mV/decade limit posed by conventional CMOS. A steeper subthreshold swing implies improved On/Off ratios facilitating aggressive voltage scaling with reduced subthreshold leakage and other short channel effects. This research work used positive aspect of both CMOS and emerging nano-electronic device CNFET in a hybrid approach towards the design of ultra-low power circuits.

6.2 Summary of Results and Contributions

The outcome of the research work and contributions has been summarized in this section. The research summary has been categorized in four parts based on the contributions made and results obtained for various circuits i.e. hybrid CMOS-CNFET Voltage Controlled Oscillator (VCO), hybrid CMOS-CNFET gm-C filters,

hybrid CMOS-CNFET bandgap reference, and dual threshold voltage reference circuit.

a) Hybrid CMOS-CNFET Voltage Controlled Oscillator(VCO):

- Hybrid VCO exhibits improved linear response over wide control voltage range suitable for PLLs.
- Lower power dissipation even at the higher frequency generated for the same control voltage. 22.6 % benefit in power dissipation for hybrid as compared to CMOS LP (same frequency power dissipation)
- Frequency scaling with increasing the number of CNTs.
- Significant reduction in power dissipation with an increase in oxide thickness.
- Smaller inter CNT pitch results in a reduction in power dissipation.
- Amongst different possibilities, the chiral vector (14,0) found to provide the least amount of power dissipation for the hybrid circuit.

b) Hybrid CMOS-CNFET OTA-C Filters:

- The hybrid OTA-C filters are suitable for biomedical signal processing applications dealing with very slow or low-frequency electrical activities of the physiological signals.
- Realized filter circuits satisfy ultra-low power consumption requirement of wearable and implantable biomedical devices. The transistors used in the circuit operate in weak inversion to achieve ultra-low power consumption.
- The first order filter consumes 216nW, the second order low pass filter consumes 433nW, and second-order notch filter consumes 431nW while the fifth order elliptic filter consumes 1.4714µW.

- In addition to capacitance and transconductance variation, desired cutoffs can also be achieved by choosing the appropriate number of nanotubes.

c) Hybrid CMOS-CNFET Bandgap Reference

- The hybrid approach utilizing proven CMOS technology with an emerging CNFET technology in a complementary manner is proposed.
- The simulation results confirm the robustness of the reference for variations in temperature and power supply.
- A precision bandgap reference with a nominal output of 500mV, 6.8 ppm/°C temperature coefficient, 0.74 %/V line sensitivity, and 26µW power dissipation is presented.
- The circuit exhibits stable operation without compensating capacitors with a startup time of 240nS at 25°C.
- A PSRR of -44dB is achieved at 25°C for 1.4V power supply.
- A satisfactory 6.8 ppm/°C temperature coefficient is achieved without any special curvature compensation.

d) Dual Threshold Voltage Reference Circuit

- The voltage reference circuit exploits subthreshold conduction and threshold voltage difference between two carbon nanotube field effect transistors (CNFETs) to achieve ultra-low power consumption.
- The reference voltage, achieved by the proposed circuit was found to be immune to the V_{th} variations if the V_{th} difference between the CNFET pair was more than 0.39V.
- The circuit exhibited excellent temperature independence, a PSRR of -86dB at 10 KHz, 0.5µS settling time and achieved 203mV reference voltage while consuming only 3.4245pW.

– Monte Carlo simulations for CNT diameter variation, and inter CNT pitch variations gave σ/μ values 1.5807% and 0.0467% respectively, signifying a robust performance of the circuit.

6.3 Conclusions

The overall conclusions from the evaluation of developed hybrid circuits are summarized below.

– CNFETs are proposed as an alternative to silicon MOSFET, but in near future, it is very difficult to replace the CMOS technology because of research advancement and economic impact of CMOS based devices.

– To bridge the gap CNFET technology can be combined with proven CMOS technology resulting in hybrid CMOS-CNFET circuits which can form the basis of the variety of circuits and systems.

– Heterogeneous integration of CMOS and emerging devices is the way to sustain Moors law in future.

– Ultra low voltage operation and subthreshold operation results in significant reduction in power dissipation for the proposed hybrid circuits.

– The number of nanotubes, inter CNT pitch and chiral vector (threshold voltage), significantly govern the power dissipation of the hybrid circuits. Barring screening effect in case of very closely spaced CNTs, increasing/decreasing the CNT count proportionately increase/decrease the drive current respectively. This gives a simple way to decide optimum number of CNTs in a CNFET channel to characterize the hybrid circuit performance.

– Just like conventional CMOS, CNFETs are also prone to manufacturing variability and this results in device mismatch consisting of random

variations in device characteristics which in turn causes behavioral variation from circuit to circuit and severely affect the robustness of the hybrid circuit performance. Mixed nature of semiconducting and metallic CNTs, density variations on account of inadvertently removal of useful semiconducting CNTs, pitch and diameter variations are the major variability issues in CNFETs and CNFET based hybrid circuits.

6.4 Future Work

There remains massive scope to further optimize the performance of hybrid circuits and develop and implement novel hybrid circuits. Some of the future direction includes:

- Fabrication of proposed hybrid circuits on IC chips.
- To work on noise analysis of hybrid circuits.
- To develop system architecture for hybrid circuits.
- To compare CMOS-CNFET hybrid circuits with similar hybrid approach such as CMOS-TFET circuits.
- Simulations and further realization of hybrid circuits at sub 10nm level.

REFERENCES

[1] M. Alioto, “Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 59, no. 1, pp. 3–29, 2012.

[2] S. R. Sridhara, “Ultra-low power microcontrollers for portable, wearable, and implantable medical electronics,” in *Proceedings of the Asia and South Pacific Design Automation Conference, ASP-DAC*, 2011, pp. 556–560.

[3] C. Galup-Montoro, M. C. Schneider, and M. B. MacHado, “Ultra-low-voltage operation of CMOS analog circuits: Amplifiers, oscillators, and rectifiers,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 59, no. 12, pp. 932–936, 2012.

[4] J. A. Paradiso and T. Starner, “Energy scavenging for mobile and wireless electronics,” *IEEE Pervasive Comput.*, vol. 4, no. 1, pp. 18–27, 2005.

[5] A. M. Ionescu *et al.*, “Ultra low power: Emerging devices and their benefits for integrated circuits,” in *Technical Digest - International Electron Devices Meeting, IEDM*, 2011, pp. 378–381.

[6] M. T. Bohr and I. A. Young, “CMOS Scaling Trends and beyond,” *IEEE Micro*, vol. 37, no. 6, pp. 20–29, 2017.

[7] “Beyond CMOS,” *Int. Roadmap Devices Syst.*, 2017.

[8] S. Datta, H. Liu, and V. Narayanan, “Tunnel FET technology: A reliability perspective,” *Microelectron. Reliab.*, vol. 54, no. 5, pp. 861–874, 2014.

[9] B. H. Lee *et al.*, “Vertically Integrated Multiple Nanowire Field Effect Transistor,” *Nano Lett.*, vol. 15, no. 12, pp. 8056–8061, 2015.

[10] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, “Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect

transistors," *Phys. Rev. Lett.*, vol. 100, no. 20, p. 206803, 2008.

[11] A. Saeidi, F. Jazaeri, I. Stolichnov, and A. M. Ionescu, "Double-Gate Negative-Capacitance MOSFET with PZT Gate-Stack on Ultra Thin Body SOI: An Experimentally Calibrated Simulation Study of Device Performance," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4678–4684, 2016.

[12] M. B. Henry and L. Nazhandali, "NEMS-based functional unit power-gating: Design, analysis, and optimization," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 60, no. 2, pp. 290–302, 2013.

[13] A. A. Prager, H. C. George, A. O. Orlov, and G. L. Snider, "Experimental demonstration of hybrid CMOS-single electron transistor circuits," *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, vol. 29, no. 4, p. 41004, 2011.

[14] J. Das, S. M. Alam, and S. Bhanja, "Ultra-low power hybrid CMOS-magnetic logic architecture," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 59, no. 9, pp. 2008–2016, 2012.

[15] W. Fei, H. Yu, W. Zhang, and K. S. Yeo, "Design exploration of hybrid CMOS and memristor circuit by new modified nodal analysis," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 6, pp. 1012–1025, 2012.

[16] A. Mishra, K. K. Jha, and M. Pattanaik, "Parameter variation aware hybrid TFET-CMOS based power gating technique with a temperature variation tolerant sleep mode," *Microelectronics J.*, vol. 45, no. 11, pp. 1515–1521, 2014.

[17] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, no. 6348, pp. 56–58, 1991.

[18] S. Iijima and T. Ichihashi, "Single-shell carbon nanotubes of 1-nm diameter," *Nature*, vol. 363, no. 6430, pp. 603–605, 1993.

[19] J. Prasek *et al.*, "Methods for carbon nanotubes synthesis - Review," *J. Mater. Chem.*, vol. 21, no. 40, pp. 15872–15884, 2011.

[20] J. C. Charlier, X. Blase, and S. Roche, "Electronic and transport properties of nanotubes," *Rev. Mod. Phys.*, vol. 79, no. 2, pp. 677–732, 2007.

[21] J. N. Coleman, U. Khan, W. J. Blau, and Y. K. Gun'ko, "Small but strong: A review of the mechanical properties of carbon nanotube-polymer composites," *Carbon N. Y.*, vol. 44, no. 9, pp. 1624–1652, 2006.

[22] M. F. L. De Volder, S. H. Tawfick, R. H. Baughman, and A. J. Hart, "Carbon nanotubes: Present and future commercial applications," *Science (80-.).*, vol. 339, no. 6119, pp. 535–539, 2013.

[23] S. Abdalla, F. Al-Marzouki, A. A. Al-Ghamdi, and A. Abdel-Daiem, "Different Technical Applications of Carbon Nanotubes," *Nanoscale Res. Lett.*, vol. 10, no. 1, pp. 1–10, 2015.

[24] A. Eatemadi *et al.*, "Carbon nanotubes: Properties, synthesis, purification, and medical applications," *Nanoscale Res. Lett.*, vol. 9, no. 1, pp. 1–13, 2014.

[25] L. Cai and C. Wang, "Carbon Nanotube Flexible and Stretchable Electronics," *Nanoscale Res. Lett.*, vol. 10, no. 1, pp. 1–21, 2015.

[26] K. Banerjee, H. Li, and N. Srivastava, "Current status and future perspectives of carbon nanotube interconnects," in *2008 8th IEEE Conference on Nanotechnology, IEEE-NANO*, 2008, pp. 432–436.

[27] H. J. Li, W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Phys. Rev. Lett.*, vol. 95, no. 8, p. 86601, 2005.

[28] M. K. Majumder, N. D. Pandya, B. K. Kaushik, and S. K. Manhas, "Analysis of MWCNT and bundled SWCNT interconnects: Impact on crosstalk and area," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1180–1182, 2012.

[29] H. Li, W. Y. Yin, K. Banerjee, and J. F. Mao, "Circuit modeling and performance analysis of multi-walled carbon nanotube interconnects," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1328–1337, 2008.

[30] H. Li, C. Xu, and K. Banerjee, "Carbon nanomaterials: The ideal interconnect technology for next-generation ICs," *IEEE Des. Test Comput.*, vol. 27, no. 4, pp. 20–31, 2010.

[31] H.-S. P. Wong and D. Akinwande, "Carbon nanotube field-effect transistors," in *Carbon Nanotube and Graphene Device Physics*, Cambridge: Cambridge University Press, 2010, pp. 191–232.

[32] A. D. Franklin *et al.*, "Carbon nanotube complementary wrap-gate transistors," *Nano Lett.*, vol. 13, no. 6, pp. 2490–2495, 2013.

[33] V. K. Sangwan, V. W. Ballarotto, M. S. Fuhrer, and E. D. Williams, "Facile fabrication of suspended as-grown carbon nanotube devices," *Appl. Phys. Lett.*, vol. 93, no. 11, p. 113112, 2008.

[34] S. J. Wind, M. Radosavljević, J. Appenzeller, and P. Avouris, "Transistor structures for the study of scaling in carbon nanotubes," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 21, no. 6, pp. 2856–2859, 2003.

[35] M. H. Yang *et al.*, "Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 88, no. 11, p. 113507, 2006.

[36] L. M. Peng, Z. Zhang, and S. Wang, "Carbon nanotube electronics: Recent advances," *Mater. Today*, vol. 17, no. 9, pp. 433–442, 2014.

[37] J. Si *et al.*, "Scalable Preparation of High-Density Semiconducting Carbon

Nanotube Arrays for High-Performance Field-Effect Transistors," *ACS Nano*, vol. 12, no. 1, pp. 627–634, 2018.

[38] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application - Part II: Full device model and circuit performance benchmarking," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3195–3205, 2007.

[39] A. U. Alam, C. M. S. Rogers, N. Paydavosi, K. D. Holland, S. Ahmed, and M. Vaidyanathan, "RF linearity potential of carbon-nanotube transistors versus MOSFETs," *IEEE Trans. Nanotechnol.*, vol. 12, no. 3, pp. 340–351, 2013.

[40] I. Meric, V. Caruso, R. Caldwell, J. Hone, K. L. Shepard, and S. J. Wind, "Hybrid carbon nanotube-silicon complementary metal oxide semiconductor circuits," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, vol. 25, no. 6, pp. 2577–2580, 2007.

[41] F. Ali Usmani and M. Hasan, "Carbon nanotube field effect transistors for high performance analog applications: An optimum design approach," *Microelectronics J.*, vol. 41, no. 7, pp. 395–402, 2010.

[42] D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H. Wong, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," *IEEE Trans. Nanotechnol.*, vol. 7, no. 5, pp. 636–639, 2008.

[43] T. S. Cho, K. Lee, T. Pan, J. Kong, and A. P. Chandrakasan, "Design and Characterization of CNT-CMOS Hybrid Systems," *MTL Annu. Res. Rep.*, 2007.

[44] K. K. Kim, Y. Bin Kim, and K. Choi, "Hybrid CMOS and CNFET power

gating in ultralow voltage design," *IEEE Trans. Nanotechnol.*, vol. 10, no. 6, pp. 1439–1448, 2011.

[45] M. H. Moaiyeri, A. Jahanian, and K. Navi, "Comparative Performance Evaluation of Large FPGAs with CNFET-and CMOS-based Switches in Nanoscale," *Nano-Micro Lett*, vol. 3, no. 3, pp. 178–188, 2011.

[46] Y. Zhou, S. Thekkel, and S. Bhunia, "Low power FPGA design using hybrid CMOS-NEMS approach," in *Proc. Intl. Symp. Low Power Electronics and Design*, 2007, pp. 14–19.

[47] R. S. Chakraborty, S. Narasimhan, and S. Bhunia, "Hybridization of CMOS with CNT-based nano-electromechanical switch for low leakage and robust circuit design," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 54, no. 11, pp. 2480–2488, 2007.

[48] M. M. Shulaker *et al.*, "Three-dimensional integration of nanotechnologies for computing and data storage on a single chip," *Nature*, vol. 547, no. 7661, pp. 74–78, 2017.

[49] M. M. Shulaker, K. Saraswat, H. S. P. Wong, and S. Mitra, "Monolithic three-dimensional integration of carbon nanotube FETs with silicon CMOS," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2014, pp. 1–2.

[50] M. M. Shulaker *et al.*, "Monolithic 3D integration of logic and memory: Carbon nanotube FETs, resistive RAM, and silicon FETs," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2015, p. 27.4.1-27.4.4.

[51] P. A. Gargini, "How to Successfully Overcome Inflection Points, or Long Live Moore's Law," *Comput. Sci. Eng.*, vol. 19, no. 2, pp. 51–62, 2017.

[52] M. M. S. Aly *et al.*, "Energy-efficient abundant-data computing: The N3XT 1,000," *Computer (Long. Beach. Calif).*, vol. 48, no. 12, pp. 24–33, 2015.

[53] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, no. 17, pp. 2447–2449, 1998.

[54] N. Patil *et al.*, "Wafer-scale growth and transfer of aligned single-walled carbon nanotubes," *IEEE Trans. Nanotechnol.*, vol. 8, no. 4, pp. 498–504, 2009.

[55] S. Kumar Sinha and S. Chaudhury, "Analysis of different parameters of channel material and temperature on threshold voltage of CNTFET," *Mater. Sci. Semicond. Process.*, vol. 31, pp. 431–438, 2015.

[56] A. K. Kureshi and M. Hasan, "Performance comparison of CNFET- and CMOS-based 6T SRAM cell in deep submicron," *Microelectronics J.*, vol. 40, no. 6, pp. 979–982, 2009.

[57] H. Shahidipour, Y. Zhong, A. Ahmadi, and K. Maharatna, "Effects of CNT diameter variability on a CNFET-based SRAM," in *IEEE Asia-Pacific Conference on Circuits and Systems, Proceedings, APCCAS*, 2010, pp. 971–974.

[58] M. M. Shulaker *et al.*, "Carbon nanotube computer," *Nature*, vol. 501, no. 7468, pp. 526–530, 2013.

[59] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: model of the intrinsic channel region," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.

[60] J. M. Chang and M. Pedram, "Energy minimization using multiple supply

voltages," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 5, no. 4, pp. 436–443, 1997.

[61] V. Stojanovic, D. Markovic, B. Nikolic, M. A. Horowitz, and R. W. Brodersen, "Energy–delay tradeoffs in combinational logic using gate sizing and supply voltage optimization," in *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, 2002, pp. 211–214.

[62] R. Rogenmoser and H. Kaeslin, "The impact of transistor sizing on power efficiency in submicron CMOS circuits," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 1142–1145, 1997.

[63] N. S. Kim, T. Kgil, K. Bowman, V. De, and T. Mudge, "Total power-optimal pipelining and parallel processing under process variations in nanometer technology," in *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, ICCAD*, 2005, pp. 534–539.

[64] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[65] A. Sathanur, L. Benini, A. Macii, E. Macii, and M. Poncino, "Row-based power-gating: A novel sleep transistor insertion methodology for leakage power optimization in nanometer CMOS circuits," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 3, pp. 469–482, 2011.

[66] H. Im, T. Inukai, H. Gomyo, T. Hiramoto, and T. Sakurai, "VTCMOS Characteristics and Its Optimum Conditions Predicted by a Compact Analytical Model," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 11, no. 5, pp. 755–761, 2003.

[67] J. W. Tschanz *et al.*, "Adaptive body bias for reducing impacts of die-to-die

and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, 2002.

[68] M. C. Johnson, D. Somasekhar, L. Y. Chiou, and K. Roy, "Leakage control with efficient use of transistor stacks in single threshold CMOS," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 10, no. 1, pp. 1–5, 2002.

[69] A. Jalan and M. Khosla, "Analysis of leakage power reduction techniques in digital circuits," in *Proceedings - 2011 Annual IEEE India Conference: Engineering Sustainable Solutions, INDICON-2011*, 2011, pp. 1–4.

[70] J. C. Park and V. J. Mooney, "Sleepy stack leakage reduction," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 14, no. 11, pp. 1250–1263, 2006.

[71] R. Sarpeshkar, *Ultra low power bioelectronics: Fundamentals, biomedical applications, and Bio-Inspired systems*, vol. 9780521857. Cambridge: Cambridge University Press, 2010.

[72] S. D. Pable and M. Hasan, "Interconnect design for subthreshold circuits," *IEEE Trans. Nanotechnol.*, vol. 11, no. 3, pp. 633–639, 2012.

[73] S. F. Wang, "Low-voltage, full-swing voltage-controlled oscillator with symmetrical even-phase outputs based on single-ended delay cells," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 23, no. 9, pp. 1801–1807, 2015.

[74] B. Li, Y. Zhai, B. Yang, T. Salter, M. Peckerar, and N. Goldsman, "Ultra low power phase detector and phase-locked loop designs and their application as a receiver," *Microelectronics J.*, vol. 42, no. 2, pp. 358–364, 2011.

[75] P. Kamalinejad, K. Keikhosravy, R. Molavi, S. Mirabbasi, and V. Leung, "An ultra-low-power CMOS voltage-controlled ring oscillator for passive RFID tags," in *New Circuits and Systems Conference (NEWCAS),IEEE 12th International*, 2014, pp. 456–459.

[76] G. Li and E. Afshari, "A low-phase-noise multi-phase oscillator based on left-handed LC-ring," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1822–1833, 2010.

[77] L. Sun, L. Tang, W. P. Jing, and J. Xia, "CMOS ring VCO for UHF RFID readers," *J. China Univ. Posts Telecommun.*, vol. 17, no. 3, pp. 20–23, 2010.

[78] E. Kougianos and S. P. Mohanty, "Impact of gate-oxide tunneling on mixed-signal design and simulation of a nano-CMOS VCO," *Microelectronics J.*, vol. 40, no. 1, pp. 95–103, 2009.

[79] R. Ganesan, J. Krumm, K. Ludwig, and M. Glesner, "Investigation of voltage-controlled oscillator circuits using organic thin-film transistors (OTFT) for use in VCO-based analog-to-digital converters," *Solid. State. Electron.*, vol. 93, pp. 8–14, 2014.

[80] M. M. Shulaker, T. F. Wu, M. M. Sabry, H. Wei, H.-S. Philip Wong, and S. Mitra, "Monolithic 3D Integration: A Path from Concept to Reality," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2015*, 2015, pp. 1197–1202.

[81] D. Devi, P. Rakesh, and V. Rakesh, "Impact of scaling gate insulator thickness on the performance of carbon nanotube field effect transistors (CNTFETs)," *J. Nano-and Electron. Phys.*, vol. 5, no. 2, pp. 2014–1, 2013.

[82] C. Kshirsagar, H. Li, T. E. Kopley, and K. Banerjee, "Accurate Intrinsic Gate Capacitance Model for Carbon Nanotube-Array Based FETs Considering Screening Effect," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1408–1411, 2008.

[83] R. K. Ranjan, S. P. Yalla, S. Sorya, and S. K. Paul, "Active comb filter using operational transconductance amplifier," *Act. Passiv. Electron. Components*,

pp. 1–6, 2014.

[84] J. Duan, C. Lan, W. Xu, and B. Wei, "An OTA-C filter for ECG acquisition systems with highly linear range and less passband attenuation," *J. Semicond.*, vol. 36, no. 5, p. 55006, 2015.

[85] S. Y. Peng *et al.*, "A Power-Efficient Reconfigurable OTA-C Filter for Low-Frequency Biomedical Applications," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 2, pp. 543–555, 2018.

[86] J. Jang, J. Lee, N. Choi, and Y. K. Song, "16 channel ultralow power analog front-end for an implantable neural recording microsystem," *IDEC J. Integr. Circuits Syst.*, vol. 2, no. 1, pp. 46–52, 2016.

[87] A. Deo, S. K. Pandey, A. Joshi, S. K. Sharma, and H. Shrimali, "Design of a Third Order Butterworth G m-C Filter for EEG Signal Detection Application," in *2018 25th International Conference Mixed Design of Integrated Circuits and System(MIXDES)*, 2018, pp. 361–365.

[88] K. A. Ng, E. Greenwald, Y. P. Xu, and N. V. Thakor, "Implantable neurotechnologies: a review of integrated circuit neural amplifiers," *Med. Biol. Eng. Comput.*, vol. 54, no. 1, pp. 45–62, 2016.

[89] J. G. Webster, *Medical Instrumentation Application and Design,* 4th ed. Boston: Wiley Global Education, 2009.

[90] C. Sawigun and W. A. Serdijn, "A modular transconductance reduction technique for very low-frequency G m-C filters," in *ISCAS 2012 - 2012 IEEE International Symposium on Circuits and Systems*, 2012, pp. 1183–1186.

[91] N. Habib, M. Muhammad, J. P. Bickford, J. Safran, A. Y. Ginawi, and F. J. Towler, "Deep Trench Capacitor in Three Dimensional Through Silicon via Keepout Area for Electrostatic Discharge Protection," *IEEE Trans. Semicond.*

Manuf., vol. 29, no. 4, pp. 292–298, 2016.

[92] A. Aminulloh, V. Kumar, S. M. Yang, and G. Sheu, “Novel structure of deep trench capacitor with higher breakdown and higher capacitance density for Low Dropout Voltage regulator,” in *Proceedings of the International Conference on Power Electronics and Drive Systems*, 2013, pp. 389–392.

[93] B. Kim, W. Xu, and C. H. Kim, “A supply-noise sensitivity tracking PLL in 32 nm SOI featuring a deep trench capacitor based loop filter,” *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1017–1026, 2014.

[94] L. Sun, Y. Chen, and K. Sun, “System integration using silicon-based integrated passive device technology,” in *Radio-Frequency Integration Technology (RFIT), 2012 IEEE International Symposium on*, 2012, pp. 98–100.

[95] H. Johari and F. Ayazi, “High-density embedded deep trench capacitors in silicon with enhanced breakdown voltage,” *IEEE Trans. Components Packag. Technol.*, vol. 32, no. 4, pp. 808–815, 2009.

[96] X. Qian, Y. P. Xu, and X. Li, “A CMOS continuous-time low-pass notch filter for EEG systems,” *Analog Integr. Circuits Signal Process.*, vol. 44, no. 3, pp. 231–238, 2005.

[97] M. S. Ansari, R. Sinha, and S. Khot, “Ultra-low power 50/60Hz notch filter for biomedical signal acquisition using 32nm±0.15 V Bulk-Driven subthreshold CMOS OTAs,” in *Electrical and Electronic Engineering (ICEEE), 2017 4th International Conference on*, 2017, pp. 309–313.

[98] R. H. Chowdhury, M. B. Reaz, M. A. B. M. Ali, A. A. Bakar, K. Chellappan, and T. G. Chang, “Surface electromyography signal processing and classification techniques,” *Sensors (Switzerland)*, vol. 13, no. 9, pp. 12431–

12466, 2013.

[99] E. Rodriguez-Villegas, A. Yúfera, and A. Rueda, "A 1.25-V micropower Gm-C filter based on FGMOS transistors operating in weak inversion," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 100–111, 2004.

[100] P. Bruschi, N. Nizza, F. Pieri, M. Schipani, and D. Cardisciani, "A fully integrated single-ended 1.5-15-Hz low-pass filter with linear tuning law," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1522–1528, 2007.

[101] Y. C. Lee, W. Y. Hsu, T. T. Huang, and H. Chen, "A compact Gm-C filter architecture with an ultra-low corner frequency and high ground-noise rejection," in *2013 IEEE Biomedical Circuits and Systems Conference, BioCAS 2013*, 2013, pp. 318–321.

[102] S. Y. Lee and C. J. Cheng, "Systematic design and modeling of a OTA-C filter for portable ECG detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 1, pp. 53–64, 2009.

[103] B. Ma and F. Yu, "A novel 1.2-V 4.5-ppm/°C curvature-compensated CMOS bandgap reference," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 61, no. 4, pp. 1026–1035, 2014.

[104] C. M. Andreou, S. Koudounas, and J. Georgiou, "A novel wide-temperature-range, 3.9 ppm/° C CMOS bandgap reference circuit," *IEEE J. Solid State Circuits*, vol. 47, no. 2, pp. 574–581, 2012.

[105] K. N. Leung, P. K. T. Mok, and C. Y. Leung, "A 2-V 23-μA 5.3-ppm/°C curvature-compensated CMOS bandgap voltage reference," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 561–564, 2003.

[106] K. K. Lee, T. S. Lande, and P. D. Hafliger, "A Sub-μW bandgap reference circuit with an inherent curvature-compensation property," *IEEE Trans.*

Circuits Syst. I Regul. Pap., vol. 62, no. 1, pp. 1–9, 2015.

[107] R. T. Perry, S. H. Lewis, A. P. Brokaw, and T. R. Viswanathan, "A 1.4 v supply CMOS fractional bandgap reference," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2180–2185, 2007.

[108] D. Hilbiber, "A new semiconductor voltage standar," in *Solid-State Circuits Conference. Digest of Technical Papers. 1964 IEEE International*, 1964, pp. 32–33.

[109] R. J. Widlar, "New developments in ic voltage regulators," *IEEE J. Solid-State Circuits*, vol. 6, no. 1, pp. 2–7, 1971.

[110] K. E. Kuijk, "A Precision Reference Voltage Source," *IEEE J. Solid-State Circuits*, vol. 8, no. 3, pp. 222–226, 1973.

[111] A. P. Brokaw, "A Simple Three-Terminal Three-Terminal IC Bandgap Reference," *IEEE J. Solid-State Circuits*, vol. 9, no. 6, pp. 388–393, 1974.

[112] B. S. Song and P. R. Gray, "A Precision Curvature-Compensated CMOS Bandgap Reference," *IEEE J. Solid-State Circuits*, vol. 18, no. 6, pp. 634–643, 1983.

[113] E. A. Vittoz and O. Neyroud, "A Low-Voltage CMOS Bandgap Reference," *IEEE J. Solid-State Circuits*, vol. 14, no. 3, pp. 573–579, 1979.

[114] H. Banba *et al.*, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *JSSC*, vol. 34, no. 5, pp. 670–674, 1999.

[115] K. N. Leung and P. K. T. Mok, "A sub-1-V 15-ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, 2002.

[116] A. Pierazzi, A. Boni, and C. Morandi, "Band-gap references for near 1-V operation in standard CMOS technology," in *Custom Integrated Circuits,*

2001, IEEE Conference on., 2001, pp. 463–466.

[117] P. Malcovati, F. Maloberti, C. Fiocchi, and M. Pruzzi, “Curvature-compensated BiCMOS bandgap with 1-V supply voltage,” *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1076–1081, 2001.

[118] J. H. Li, X. B. Zhang, and M. Y. Yu, “A 1.2-V piecewise curvature-corrected bandgap reference in 0.5 µm CMOS process,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 6, pp. 1118–1122, 2011.

[119] G. De Vita and G. Iannaccone, “A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator,” *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536–1542, 2007.

[120] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutrì, “A low-voltage low-power voltage reference based on subthreshold MOSFETs,” *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 151–154, 2003.

[121] M. Seok, G. Kim, D. Blaauw, and D. Sylvester, “A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 v,” *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2534–2545, 2012.

[122] D. Albano, F. Crupi, F. Cucchi, and G. Iannaccone, “A picopower temperature-compensated, subthreshold CMOS voltage reference,” *Int. J. Circuit Theory Appl.*, vol. 42, no. 12, pp. 1306–1318, 2014.

[123] A. Lin *et al.*, “Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs,” *IEEE Trans. Nanotechnol.*, vol. 8, no. 1, pp. 4–9, 2009.

[124] N. Patil, J. Deng, A. Lin, H.-S. P. Wong, and S. Mitra, “Design methods for misaligned and mispositioned carbon-nanotube immune circuits,” *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 27, no. 10, pp. 1725–1736,

2008.

[125] C. G. Almudever and A. Rubio, “Variability and reliability analysis of CNFET technology: Impact of manufacturing imperfections,” *Microelectron. Reliab.*, vol. 55, no. 2, pp. 358–366, 2015.

[126] C. García and A. Rubio, “Manufacturing variability analysis in carbon nanotube technology: A comparison with bulk CMOS in 6T SRAM scenario,” in *Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2011*, 2011, pp. 249–254.

[127] L. Qu, F. Du, and L. Dai, “Preferential syntheses of semiconducting vertically aligned single-walled carbon nanotubes for direct use in FETs,” *Nano Lett.*, vol. 8, no. 9, pp. 2682–2687, 2008.

[128] H. Wei *et al.*, “Efficient metallic carbon nanotube removal readily scalable to wafer-level VLSI CNFET circuits,” in *Digest of Technical Papers - Symposium on VLSI Technology*, 2010, pp. 237–238.

[129] L. An, Q. Fu, C. Lu, and J. Liu, “A simple chemical route to selectively eliminate metallic carbon nanotubes in nanotube network devices,” *J. Am. Chem. Soc.*, vol. 126, no. 34, pp. 10520–10521, 2004.

[130] X. Liu *et al.*, “Detailed analysis of the mean diameter and diameter distribution of single-wall carbon nanotubes from their optical response,” *Phys. Rev. B - Condens. Matter Mater. Phys.*, vol. 66, no. 4, pp. 454111–454118, 2002.

Appendix A

Publications on Research Work

1. S.B. Rahane, A. K. Kureshi, and S. D. Pable. "A hybrid CMOS-CNFET, 1.4-V 6.8-ppm/° C bandgap reference circuit." in India Conference (INDICON), 2015 Annual IEEE, pp. 1-5. IEEE, 2015. (ISSN: 2325-9418, DOI: 10.1109/INDICON.2015.7443249,Available-online https://ieeexplore.ieee.org/abstract/document/7443249/, Scopus Source Record id (2017) 21100784360)
2. S.B. Rahane, A. K. Kureshi, and G.K. Kharate. "OTA-C filters for biomedical signal processing applications using hybrid CMOS-CNFET technology" Accepted for presentation and publication in proceedings of IEEE 2018 International Conference on Intelligent and Innovative Computing Applications (IEEE - ICONIC 2018), Mauritius.
3. S.B. Rahane, and A. K. Kureshi. "A low power and linear voltage controlled oscillator using hybrid CMOS-CNFET technology." International Journal of Applied Engineering Research, vol. 12, no. 9 (2017), pp. 1969-1973.(ISSN: 0973-4562,Available-online https://www.ripublication.com/ijaer17/ijaerv12n9_29.pdf, Scopus Source Record id (2017) 21100217234)
4. S.B. Rahane, A. K. Kureshi, and G.K. Kharate. "Ultra-low power voltage reference circuit utilizing a threshold voltage difference between two CNFETs" ICTACT Journal on Microelectronics, vol. 4, no. 1 (2018), pp.531-536. (ISSN 2395-1680, DOI 0.21917/ijme.2018.0093, Available online http://ictactjournals.in/paper/IJME_Vol_4_Iss_1_Paper_5_531_536.pdf)
5. S.B. Rahane, and A. K. Kureshi. "Hybrid CMOS and CNFET low pass gm-C filters." International Journal of Research in Electronics and Computer Engineering, vol. 5, no. 4 (2017), pp. 426-430.(ISSN: 2348-2281, Available online http://www.i2or-ijrece.com/vol.-5-issue-4--version-2-.html)
6. S.B. Rahane, and A. K. Kureshi."A review of conventional and emerging power gating techniques for leakage power reduction" International Journal of Innovative Research in Science, Engineering and Technology, vol. 3, no.4 (2014),pp. 420-427.(ISSN: 2319–8753, Available online https://www.ijirset.com)

Appendix B

Analytical Expressions for Ballistic NCNFET[†]

(1) $$I_{ON} \approx \frac{k_B T}{e.R_q} ln\left[1 + \ e^{(2e\varphi_s - E_g)/2k_B T}\right]$$

(2) $$I_D = \frac{k_B T}{e.R_q}\left\{ln\left[1 + \ e^{(2e\varphi_s - E_g)/2k_B T}\right] - ln\left[1 + e^{(2e\varphi_s - 2e\alpha V_D - E_g)/2k_B T}\right]\right\}$$

(3) $$I_{sth} \approx \frac{k_B T}{e.R_q}\left[e^{(2eV_G - E_g)/2k_B T} - e^{(2eV_G - 2e\alpha V_D - E_g)/2k_B T}\right]$$

(4) $$V_T \approx k_B T \ ln\left\{\frac{1}{12} e^{(E_g + e\alpha V_D)/2k_B T}\left[\sqrt{e^{(e\alpha V_D)/k_B T} + 24} - e^{(e\alpha V_D)/2k_B T}\right]\right\}$$

(5) $$g_m = \frac{\partial I_D}{\partial V_G} = \left[\frac{1}{1 + e^{(2e\varphi_s - 2e\alpha V_D - E_g)/2k_B T}} - \frac{1}{1 + e^{(2e\varphi_s - E_g)/2k_B T}}\right]\frac{1}{R_q}\frac{\partial \varphi_S}{\partial V_G}$$

(6) $$g_{ds} = \frac{\partial I_D}{\partial V_D} = \frac{\propto}{R_q}\left[1 + e^{(E_g + 2e\alpha V_D - 2e\varphi_s)/2k_B T}\right]^{-1}$$

† H.-S. P. Wong and D. Akinwande, “Carbon nanotube field-effect transistors,” in *Carbon Nanotube and Graphene Device Physics*, Cambridge: Cambridge University Press, 2010, pp. 191–232.

Appendix C
Key CNFET Model Parameters[†]

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

[†] J. Deng and H. S. P. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: model of the intrinsic channel region," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3186–3194, 2007.